THE UNIVERSITY *of* EDINBURGH

Microelectromechanical systems for biomimetical application

Rhonira Latif

A thesis submitted for the degree of Doctor of Philosophy.

The University of Edinburgh

December 2012

Abstract

The application of adaptive micro-electro-mechanical systems (MEMS) device in biologically-inspired cochlear model (cochlear biomodel) has been seen as a preferable approach to mimic closely the human cochlear response. The thesis focuses on the design and fabrication of resonant gate transistor (RGT) device applied towards the development of RGT cochlear biomodel. An array of RGT devices can mimic the cochlea by filtering the sound input signals into multiple electrical outputs. The RGT device consists of two main components; a) the MEMS bridge gate structure that transduces the sound input into mechanical vibrations and b) the channel with source/drain regions underneath the bridge gate structure that transduce the mechanical vibrations into electrical signals. The created mathematical model for RGT calculates the electrical outputs that are suited for neural spike coding. The neuromorphic auditory system is proposed by integrating the RGT devices with the spike event interface circuits. The novelty of the system lies in the adaptive characteristics of the RGT devices that can self-tune the frequency and sensitivity using the feedback control signals from the neuromorphic circuits.

The bridge gates have been designed to cover the audible frequency range signals of $20\ Hz - 20\ kHz$. Aluminium and tantalum have been studied as the material for the bridge gate structure. The fabrication of a bridge gate requires a gentle etch release technique to release the structure from a sacrificial layer. The downstream etch release technique employing oxygen/nitrogen plasma has been introduced and characterised. In the first iteration, aluminium bridge gates have been fabricated. The presence of tensile stress within aluminium had caused the aluminium bridge gates of length $> 1\ mm$ to collapse. In order to address this issue, tantalum bridge gates have been fabricated in the second iteration. Straight tantalum bridge gates in tensile stress and buckled tantalum bridge gates in compressive stress have been characterised. The frequency range of $550\ Hz - 29.4\ kHz$ has been achieved from the fabricated tantalum bridge gates of length $0.57\ mm - 5.8\ mm$.

The channel and source/drain regions have been fabricated and integrated with the aluminium or tantalum bridge gate structures to create the RGTs. In this study, the *n*-channel and *p*-channel resonant gate transistor (*n*-RGT and *p*-RGT) have been considered. In *n*-RGT, phosphorus ions are implanted to form the source/drain regions. High subthreshold currents have been measured from the *n*-RGTs. Thus, *p*-RGTs have been employed with considerably small subthreshold current. In *p*-RGT, boron ions are implanted to form the source/drain regions. The threshold voltage, transconductance and subthreshold current for both *n*-channel and *p*-channel resonant gate transistor devices have been characterised. In this work, the channel conductance of the *n*-RGT and *p*-RGT devices has been modulated successfully and the sensitivity tuning within the audible frequency range has been achieved from the tantalum bridge gates of the *p*-RGT devices. The characterisation and optimisation of the resonant gate transistor provide the first step towards the development of the adaptive RGT cochlear biomodel for the neuromorphic auditory system application.

Declaration of originality

I hereby declare that the research recorded in this thesis and the thesis itself was composed originated entirely by myself in the School of Engineering and Electronics at The University of Edinburgh.

List your exceptions here and sign before your printed name

Rhonira Latif

Contents

List of symbols

l_b	Bridge gate length
w_b	Bridge gate width
t_b	Bridge gate thickness
A_b	Cross sectional area of the bridge gate, $w_b \times t_b$
W_c	Channel width
L_c	Channel length
A_c	Area of the channel region, $W_c \times L_c$
E	Young's modulus
ρ	density
F	Net input force applied on the bridge gate
F_e	Attractive electrostatic force
F_m	Mechanical restoration force
x	Bridge gate vibration displacement
ω_0	Mechanical resonant radial frequency
m	Effective bridge gate mass
b	Damping coefficient
k	Elastic restoring coefficient
ζ	Damping ratio
Q_3	Quality factor at $-3\ dB$
Q_{10}	Quality factor at $-10\ dB$
d_i	Air gap spacing between bridge gate and channel region
σ	Biaxial residual stress
σ_{tens}	Biaxial residual tensile stress
σ_{comp}	Biaxial residual compressive stress
υ	Poisson's ratio
y_c	Maximum central vertical deflection of buckled bridge gate

V_{gs}	Gate/bridge gate voltage
V_{ds}	Source-drain voltage
V_{pi}	Pull-in voltage
V_{th}	Threshold voltage
ε_0	Permittivity of air
ε_{ox}	Permittivity of silicon dioxide (gate oxide)
ε_{si}	Permittivity of silicon (substrate)
t_{ox}	Gate oxide thickness
ψ	Viscosity coefficient
C_{total}	Total capacitance per unit area
C_{air}	Air gap capacitance per unit area
C_{ox}	Gate oxide capacitance per unit area
μ	Effective mobility of charge carriers
μ_e	Effective mobility of electrons
μ_h	Effective mobility of holes
I_{ds}	Drain current
g_m	Transconductance
N_D	Phosphorus doping concentration
N_A	Boron doping concentration
λ	Channel length modulation parameter
Q_{ss}	Positive oxide charges
φ_{MS}	Metal-silicon work function
I_{th}	Subthreshold current
ρ_s	Sheet resistivity
ρ_c	Contact resistivity
R_c	Contact resistance
X_j	Junction depth
f_n	n^{th} vibrational mode
n	Mode number

E_a	Activation energy
T	Substrate temperature
k_p	Undercut etch rate

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Chapter 1: Introduction

The chapter commences with the introduction of biologically-inspired sensors in biomimetical applications. The main focus of the project will be directed on the study of human auditory system. The functionalities of cochlea in auditory system can be reproduced using micro-electro-mechanical systems (MEMS) device, in conjunction with the neuromorphic electronics. The aim of this project is to study and fabricate an artificial cochlea that is adaptive, by employing a MEMS device called the resonant gate transistor (RGT). The tuning ability of RGT and the integration of this device with neuromorphic electronics create a possibility of an operational active system that can mimic closely the mechanism of hearing. The main challenge would be to design the RGT device to have similar performance of sensing and tuning ability with the real cochlea. By mimicking the auditory system, one could help to improve the understanding of hearing mechanism, leading to accurate modelling of cochlea and thus, better application could be benefited from the model.

1.1 The biomimetical study

This section introduces biomimetical/biomimicry, the study and imitation of the biological system to solve human problems [1][2]. The living system is no different from the engineered system, where each part or sub-part of the system has been designed to perform a specific function [1]. Nature possesses complex mechanisms and incredible abilities that have been developed over billions of years. Thus, nature offers models and inspirations for designing artificial systems that can mimic its natural behaviour. An example of biomimicry is the copy of jellyfish swimming,

floating and sinking behaviours for underwater microrobots which are used for monitoring and exploring underwater environment [3].

The remarkable adaptive and sensing capabilities of the biological systems have sparked interest for new innovation of sensor technology or optimisation of the current one [1]. For instance, parasitoids fly with a scientific name of *Ormia Ochracea* possesses excellent ability of detecting sound direction within the small interaural time difference. The micromachined directional microphones have been fabricated as the sound source localisation sensor to replicate the auditory organ of the insect [4]. The biologically-inspired sensors are usually designed to have high sensitivity with low energy requirement and parallel sampling/processing of the sensory information [1].

In our research, the biomimetical study will focus on the cochlea of human auditory system. The main aim and objectives of the research will be pointed out in section 1.2.4. The anatomy and physiology of cochlea within the human auditory system will be reviewed first.

1.1.1 The behavioural studies of human auditory system

The audible frequency range that can be perceived by a normal human ear is between $20\ Hz$ to $20\ kHz$ with the intensity above the threshold of hearing ($0\ dB$) up until threshold of pain ($120\ dB$) [5][6][9]. The frequency is related to pitch of sound while the magnitude of intensity correlates to loudness. The intensity is measured in decibel scale with respect to the threshold of hearing [5][6].

The auditory system can be divided into outer, middle and inner ear sections as shown in Figure 1.1. The outer and middle ear transfer the incoming sound pressure waves towards cochlea and also distinguish the directions of the received sound. The outer and middle ear sections provide an impedance matching mechanism for a maximum transmission of sound pressure waves travelling from air to the fluid within the cochlea. In addition, the protective mechanism by the middle ear muscles reduces the ear responses to loud noises [5].

The cochlea that resides within the inner ear section is a fluid pressure sensor that transforms the travelling waves of the sound input signals into mechanical vibrations and electrical action potentials. The physiological aspects and electromechanical response of the cochlea are studied in the following section.

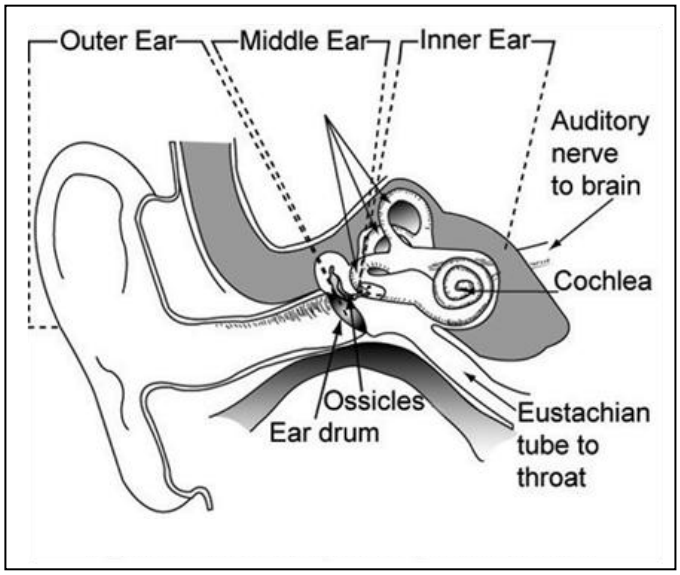
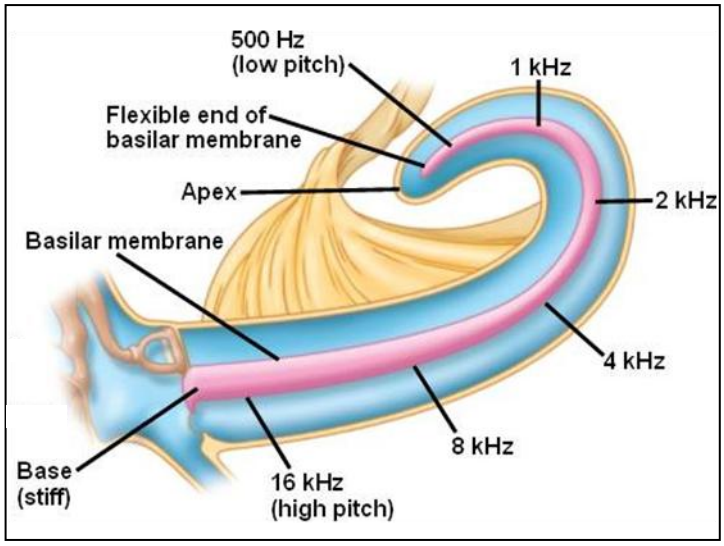


Figure 1.1 *The anatomical structure of a human auditory system showing the outer, middle and inner ear sections. The cochlea is situated within the inner ear section. Image courtesy from www.nasa.gov.*

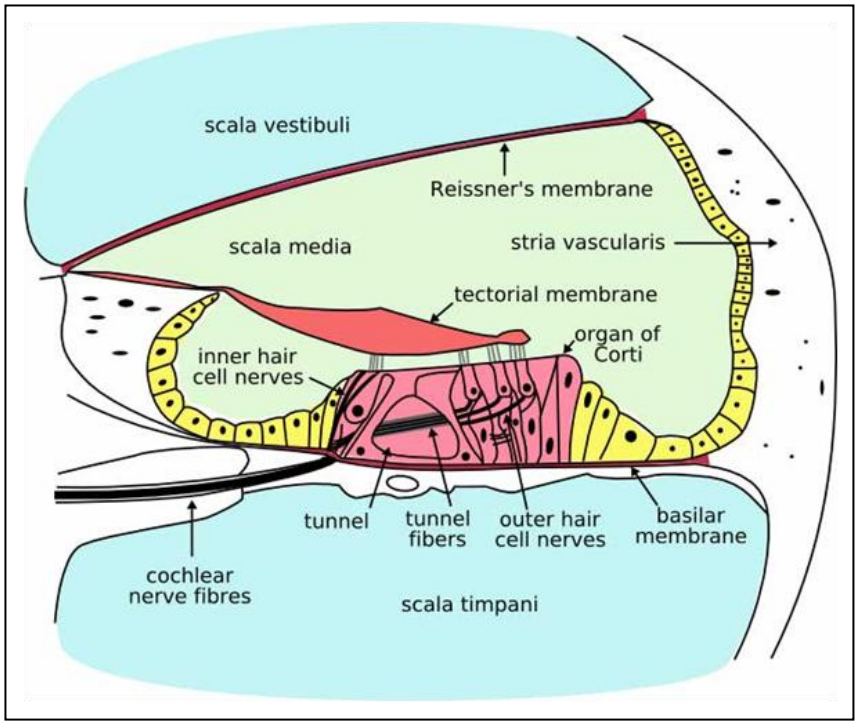
1.1.1.1 The mechanical response of basilar membrane in cochlea

The schematic diagram of a cochlea is shown in Figure 1.2(a). The cochlea is uncoiled/unrolled in Figure 1.2(b) and the cross section of the uncoiled cochlea duct is depicted in Figure 1.2(c). The motion and vibration of a membrane within the cochlea called basilar membrane (BM) are vital in the mechanics of cochlea [Figure 1.2(b)] [5][6][10]. The BM is $35\ mm$ in length, coiled, tapered in width from base ($100\ \mu m$) to apex ($500\ \mu m$) and located between scala media and scala tympani [Figure 1.2(c)][5][15]. The movement of BM depends on the frequency, amplitude and time of the travelling waves that propagate from base towards the apex of BM. The base of BM which is narrow and stiff, will respond to high frequency/high pitched sound while the broader apex which is more flexible will respond to low frequency signal [Figure 1.2(b)].

(a) Cochlea



(b) Uncoiled cochlea



(c) Cross section of the uncoiled cochlea

Figure 1.2 *(a) The schematic diagram of a cochlea. Image taken from http://discovermagazine.com/2007/jan/math. (b)The cochlear duct is depicted as uncoiled/unrolled. Image taken from http://www.nicerweb.com/bio1152/Locked/media/ch50/pitch.html. (c) A magnified cross section view of the cochlear duct. Image taken from http://www.webbooks.com/eLibrary/Medicine/Physiology/Ear/Cochlea.png.*

Each section point along the membrane corresponds to a certain resonant/natural frequency f_1 with maximum vibration amplitude. The spatial arrangement of frequency along the length of BM is called the tonotopic organisation or frequency-to-place mapping. Assuming the normalised distance from apex to base as $0 \leq \chi \leq 1$, the frequency f_1 at a distance χ from apex is given by equation 1.1 [12][11];

$$f_1(\chi) = 160(10^{2.1\chi} - 0.8) \tag{1.1}$$

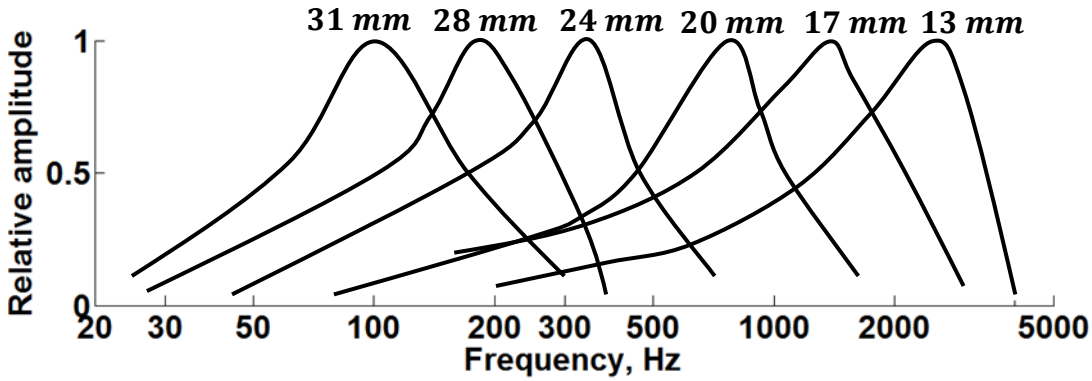
Figure 1.3(a) shows the measured frequency responses from six different section points on a basilar membrane of a human cadaver performed by von Békésy [5][6]. The sound input signals have stimulated transverse vibrations of maximum amplitudes at different values of resonant frequencies along the length of BM. Each point on the membrane works like a bandpass filter, signifying the function of the whole BM as a real-time mechanical frequency analyser for the sound input signals [9]. The measured travelling wave in BM was broadly-tuned with a quality factor of Q_{10}~0.6. The value of Q_{10} refers to the division of frequency f_1 at peak mechanical vibration to frequency bandwidth BW_{10} at 10 dB below the peak vibration [equation 1.2] [Figure 1.3(b)][18].

$$Q_{10} = \frac{f_1}{BW_{10}} \tag{1.2}$$

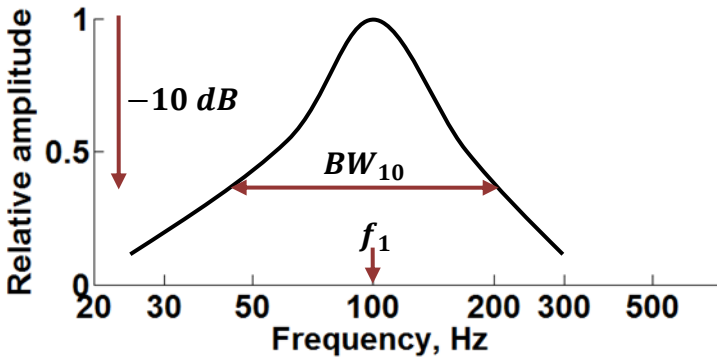
The measured small quality factor of Q_{10}~0.6 is indicative of poor frequency selectivity from the membrane. This is due to the passive mechanical response of the cochlea, as the experiments have been performed on cadavers instead of living human. Better responses with higher Q_{10}~$3 - 10$ have been measured from the BM of living animals in good physiological condition [5][6][8]. The detected better quality of frequency selectivity from a healthy and normal ear implies the occurrence of active mechanical and/or electrical mechanism within the cochlea [5][6]. The mechanism that induces this active process is still unknown.

Another important membrane is the tectorial membrane (TM) that covers the top side of the Organ of Corti [Figure 1.2(c)]. A group of researchers has found an additional wave that travels side by side in TM on top of the wave that propagates up and down

in BM [13]. They claimed that the ear can translate sounds into these two different motions simultaneously, which may explain the remarkable sensitivity of human ear that can hear sounds as quiet as whispers.



(a) The measured frequency responses from BM



(b) BW_{10} and f_1

Figure 1.3 *(a) The measured frequency responses from the basilar membrane of a cadaver. The measurement has been performed at six different positions with the distance of* $13\ mm - 31\ mm$ *from the base of the membrane. Results from von Békésy and graph reproduced from [5]. (b) The bandwidth* BW_{10} *and resonant frequency* f_1 *define the quality factor* $Q_{10} = \frac{f_1}{BW_{10}}$ *of a frequency response.*

1.1.1.2 The electrical response of hair cells in cochlea

The process flow for sound reception and analysis by the auditory system is shown in Figure 1.4. The vibration pattern of BM embodies the information regarding the frequency, amplitude and time of the sound input signals that stimulate the BM. The Organ of Corti that sits on top of BM and below TM [Figure 1.2(c)] contains

receptor cells called hair cells that transduce the occurred mechanical vibrations in BM into electrical neural signals.

Basically, the vibrations of BM will deflect/displace the hair cells. This excitation will generate 1) electrical signals within the hair cells and 2) neural spike signals that will be transmitted from the hair cells to auditory nerve fibres. There are $15\,000 - 25\,000$ hair cells that can encode the vibrations of BM into neural spike signals. The encoded neural spikes are then transmitted to brain via the nerve fibers [5][6].

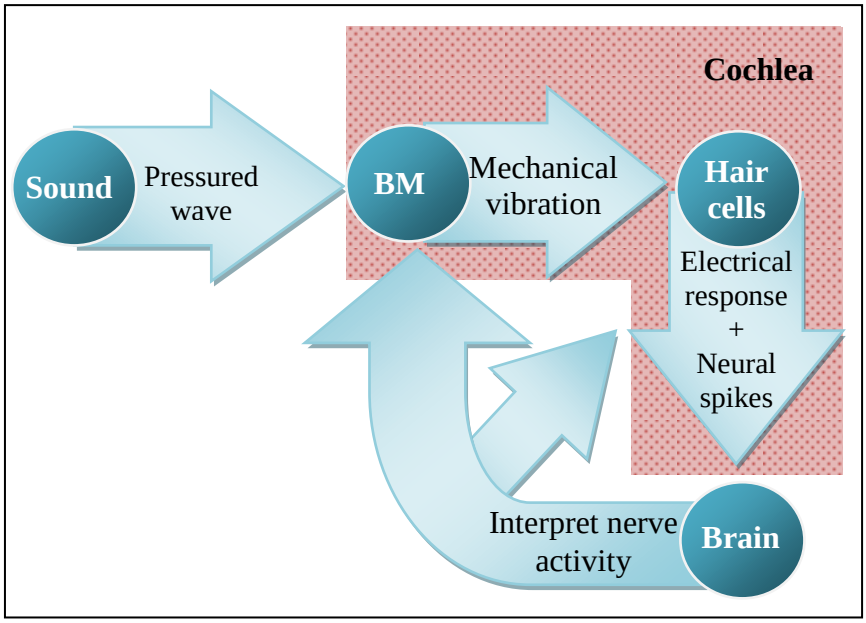


Figure 1.4 *The reception and analysis of sound by human auditory system. The transformation/transduction of sound pressure waves into neural spikes is performed by the cochlea.*

Within the hair cells, the induced electrical signals consist of AC and DC components [5][6]. The AC response within the hair cells follows the sound input stimulation waveform, like a microphone. A maximum receptor potential of 1.5 mV has been measured at 800 Hz from a hair cell of the guinea-pig cochlea [5]. The frequency response of one hair cell has been reported to possess the broadly-tuned electrical bandpass characteristic that follows closely the mechanical response of a section point in BM [5][6].

A single auditory hair cell innervates a single point in BM. This preserves the tonotopic organisation characteristics of the basilar membrane onto the auditory nerve fibres. The brain interprets the locations of nerve activity in order to find out the vibrating section points within the BM and thus figuring out the frequency of the sound input that has triggered the vibration initially. The feedback energy signals from brain to the hair cells and/or BM via the nerve fibers have been postulated to be responsible for the higher quality factor and sensitivity of a living cochlea compared to those measured from the cadavers [5][6].

1.2 Motivation and problem statement

In this section, the aim and motivation of our research are discussed. The cochlear implant is invented to aid people with hearing loss problem. It was reported that approximately 219 000 adults and children have received the implants by the end of 2010 [7]. The number of stimulating sites for the cochlear implant has been increased continuously through the years with the purpose of enabling the users to possess better hearing in noisy environment and also to discern specific tones [14]. A suitable speech processing strategy is programmed and stored within the processor of the implant by the user's personal audiologist. This hearing aid however, does not resemble the complex mechanism of human auditory system. In fact, the mechanics of cochlea has not been understood fully. If the function of human cochlea is studied properly and it can be copied, a better hearing loss correction is possible.

The actual mechanism of human cochlea remains open for discussion as there is no single verified mechanism that can explain the ear's remarkable sensitivity and selectivity towards sounds. The physical model i.e. biomodel of cochlea can be created and studied as an alternative approach of understanding the cochlear mechanism. There are three different types of cochlear biomodels which have been fabricated by others. There are fluidic, electronic and MEMS cochlear biomodels. The passive nature of the current cochlear biomodels has captured the interest in fabricating an active/adaptive cochlear biomodel which can imitate the functionalities of the real cochlea. The intensity of sound input can be controlled by

the cochlea in such a way that a human being could hear whispers in quiet environment and conversely not deafened by the ambulance's siren. Presently, the fabricated cochlear biomodels could not yet reproduce this adaptive behaviour of cochlea.

1.2.1 Fluidic cochlear biomodel

In the past decades, a large body of research on the development of the physical and mathematical models of human cochlea has been reported extensively. The very first physical model of human cochlea was developed in fluidic surroundings. Georg von Békésy used the measured data from cochleas of the cadavers to build the first fluidic cochlear biomodel [9][15]. The early designs of fluidic cochlear biomodels are passive and bulky with the size of many times bigger than the actual size of cochlea.

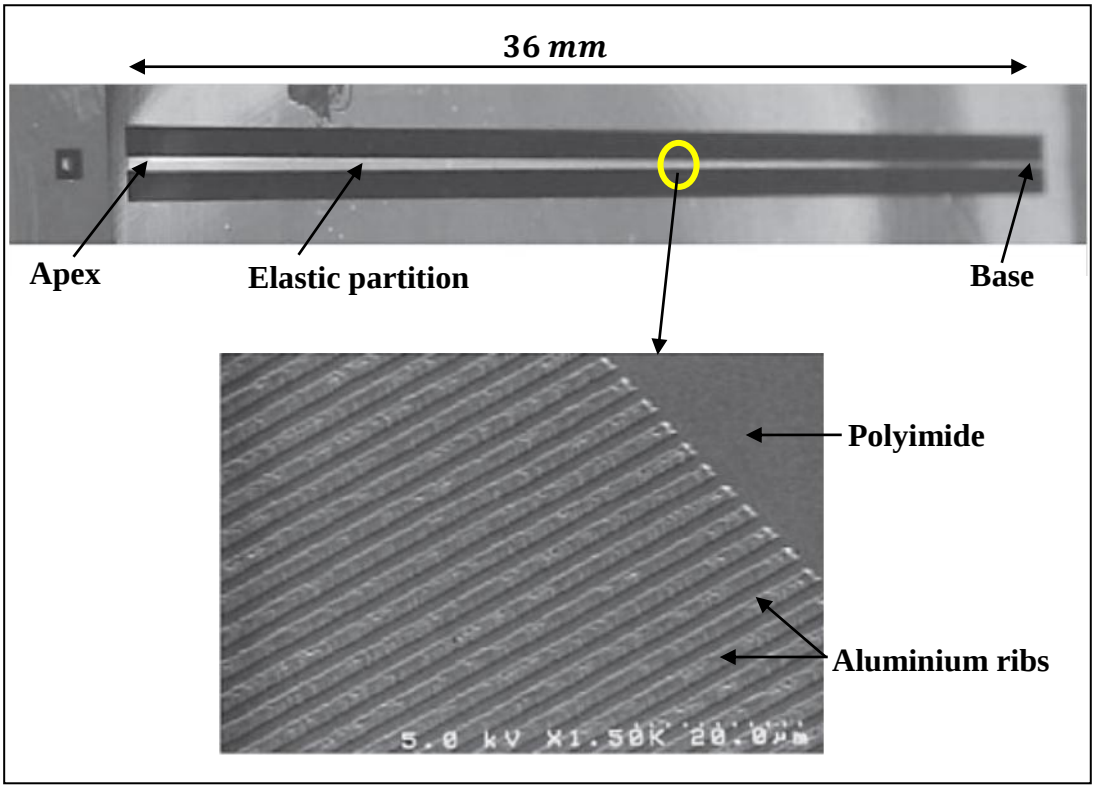


Figure 1.5 *An example of fluidic cochlear biomodel fabricated by Wittbrodt et al. The micromachined elastic partition is made of polyimide/discrete aluminium ribs to mimic the size and functional properties of BM. Image taken from[15].*

A life-sized fluidic cochlear biomodel has then been created using the available advanced technology of microfabrication [Figure 1.5] [9][15][17][16][18]. The elastic partitions and membranes with specified dimensions are micromachined from materials like silicon, silicon nitride or polyimide/aluminium to imitate the frequency-to-place mapping characteristics of the basilar membrane [9][15]. The microfabrication technology also promises future integration of electrical sensing elements into the fluidic cochlear biomodel.

1.2.2 Analogue electronics cochlear biomodel

A different type of cochlear biomodel based on the electronics circuitry has also been designed. The first analogue electronics cochlear biomodel with VLSI implementation has been created by Lyon *et al* in 1988 [19].

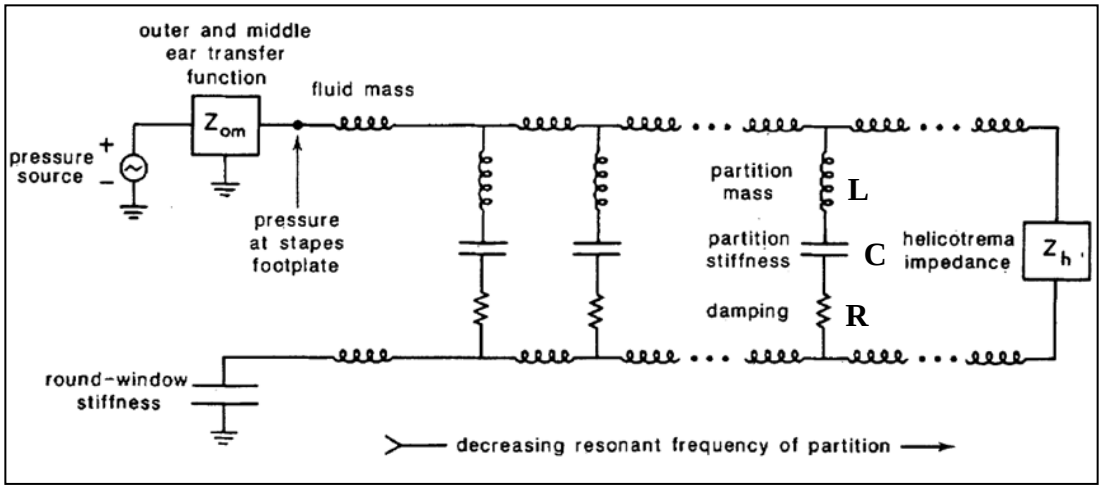


Figure 1.6 *The electrical equivalent circuit for cochlea. The series of RLC resonant circuits represent each section point in BM that corresponds to different resonant frequency f_1. Image taken from [20].*

The mathematical model of cochlea breaks the BM into sections/partitions and presumes the behaviour of each section point in terms of lumped mass, stiffness and damping. In the electrical equivalent circuit for cochlea, the lumped mass, stiffness and damping of the membrane in each section are modelled as the RLC tank resonant circuit [Figure 1.6][20]. The series of RLC resonant circuits act as bandpass filters at

different values of resonant frequency f_1 and signify the frequency-to-place mapping characteristics of the basilar membrane. The input signals are converted into multiple outputs by this bank of bandpass filters [12][19]. The damping and thus quality factor of each cochlear section can be adjusted using AC feedback [11][12]. The complex AC feedback is however difficult to be implemented for each section.

1.2.3 MEMS cochlear biomodel

Micro-electro-mechanical systems (MEMS) are mechanical devices driven by electrical means at the microscopic level. The advanced development of the microfabrication technology and the fact that the cochlea itself is an electromechanical transducer, have drawn the attention of employing MEMS in the cochlear biomodels [17][16][18]. In 1995, the MEMS resonators for examples the cantilevers or bridges have been applied in the cochlear biomodels.

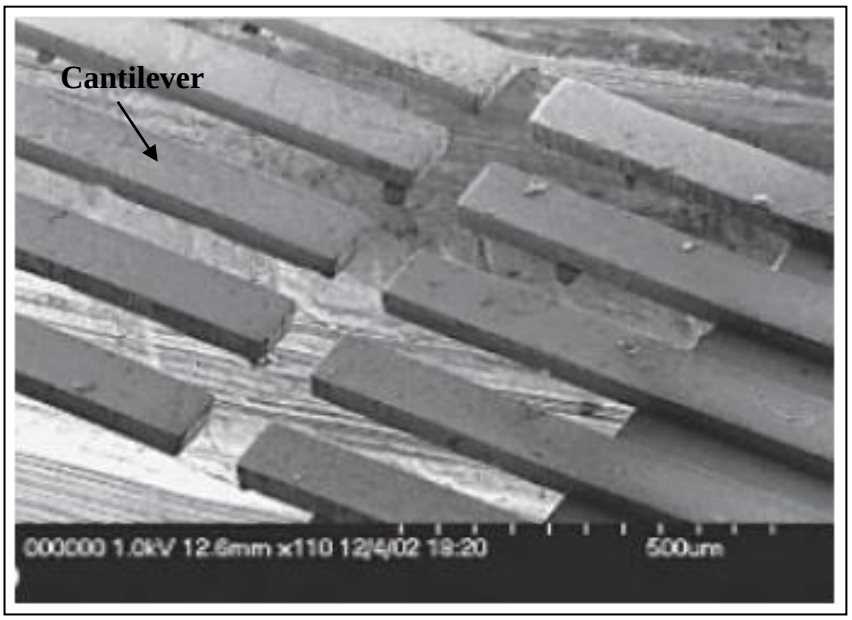


Figure 1.7 *The fabricated array of MEMS cantilevers with different length has been measured to mimic the frequency-to-place mapping characteristics of BM. Image taken from [18].*

An array of MEMS resonators, each with a specific frequency f_1, can perform the passive parallel spectral filtering in a similar manner with the basilar membrane [16][18]. In Figure 1.7, the MEMS cantilevers of different length have been

fabricated by Bachman *et al* to mimic the frequency-to-place mapping characteristics of the basilar membrane [18]. The geometrical dimensions of the MEMS resonators can be manipulated in order to attain a certain value of resonant frequency and quality factor.

1.2.3.1 Advantages of MEMS in cochlear implant

The cochlear implant transforms the sound input signals into a single electrical signal. Then, the filtering of the single electrical signal produces output signals with latency drawback. The application of multiple MEMS resonators can solve the problem. The advantage of employing an array of resonators is the instantaneous parallel spectral breakdown of the input that maintains the timing and reduces the latency of output signals [16][18].

Typically, a programmable speech processor is needed for analogue to digital conversion of the detected sound input. The researchers noticed the potentials of using the MEMS resonators to alleviate the need of a speech processor in cochlear implant. The sound input signals can be sensed directly by the MEMS resonators, bypassing the analogue to digital conversion [16][18].

1.2.3.2 Advantages of MEMS in cochlear biomodel

The introduction of MEMS in cochlear biomodel is attractive due to the small size, direct and parallel processing of the sensory information and straightforward transformation between the mechanical and electrical domain. In terms of filtering, the MEMS cochlear biomodel can be designed to have better quality factor compared to other cochlear biomodels. The sensitivity and frequency selectivity of MEMS resonator can be designed from its geometry, material properties and the medium that surrounds the resonator [16][18][10].

A computer based controller is used for producing and transmitting the feedback signals which will control the way the cochlear biomodel processes sound. Many conditions can be enforced onto the cochlear biomodel for examples, to listen to a single frequency only or the harmonically related frequencies, to decide on the time

to apply the feedback control signal and to amplify or dampen the vibration of certain frequencies. The feedback control signals can be imposed onto the MEMS cochlear biomodel simply by applying and varying the DC drive onto the resonator.

The tuning of vibration amplitude for the basilar membrane which comes from the stiffening and softening of the membrane can be correlated with the change in the elastic restoring coefficient/spring constant of the MEMS resonator due to the applied DC drive. The capability of the MEMS resonating structures to be tuned by DC drive might suggest a close imitation of the MEMS cochlear biomodel with the actual principles of the active cochlear mechanism [12]. Thus, the adaptive MEMS cochlear biomodel is pursued in this work.

1.2.4 Aim and objectives

The aim of this research is to study and mimic the behaviour of human cochlea by constructing the adaptive MEMS cochlear biomodel. The MEMS device that can sense directly the sound input signals by mechanical and electrical means is designed and the possibility of integration with neuromorphic electronics is investigated. The fabricated array of MEMS devices is expected to be able to cover the 3-decade band of frequency spectrum. The novelty of this project is the adaptive capability of the MEMS device within the MEMS cochlear biomodel integrated with the neuromorphic circuits. Each MEMS device should be able to self-control/tune the sensitivity and selectivity of the detected signal.

In summary, there are 3 objectives to be accomplished from the fabricated MEMS cochlear biomodel;

1) Audible frequency range detection ($20\ Hz - 20\ kHz$).
2) Self-controlled gain and frequency from each individual MEMS device (adaptive).
3) Suitable electrical output signal from MEMS device for neural spike coding.

The realisation of the above objectives could be achieved by employing the MEMS device called resonant gate transistor (RGT) to mimic the cochlea's functions. From here, the MEMS cochlear biomodel will be addressed as the RGT cochlear biomodel.

1.3 Methodology

In order to build the cochlear biomodel, the physiological study of the cochlea within human auditory system has been reviewed in section 1.1.1. A cochlear-inspired system should include 1) an artificial basilar membrane to detect the mechanical vibrations 2) the artificial hair cells that transform the mechanical vibrations into electrical signals 3) the neuromorphic circuit that produces neural spike signals from the detected electrical signals and 4) a computational model that processes the spikes and deliver control signals back to the artificial basilar membrane and/or hair cells. The thesis will focus on the fabrication and application of RGT device within the RGT cochlear biomodel that can satisfy 1) and 2); plus to make sure that the condition of the induced electrical output signals from 2) can be further processed by the neuromorphic circuit.

1.3.1 RGTs for MEMS cochlear biomodel

Resonant gate transistors (RGTs) are MEMS devices with the possibility of mimicking the functionalities of basilar membrane and hair cells in the cochlea. In Figure 1.8, the mechanical part of RGTs comprises an array of MEMS resonator bridges that behave as a real-time mechanical frequency analyser and copy the frequency-to-place mapping characteristics of the basilar membrane. The electrical part of RGT is the channel region between source and drain. The channels with source/drain can mimic the electrical performances of the hair cells by transducing the detected mechanical vibrations from the MEMS resonator bridges into electrical signals. The theoretical development for RGT is presented in Chapter 2.

1.3.1.1 MEMS resonators for artificial basilar membrane

The MEMS resonator in RGT is usually designed to work at a higher resonant frequency range and quality factor compared to the frequency response measured from the basilar membrane. In order to map and copy the desired response from BM, three approaches of RGT design will be taken. 1) Each of the resonator's structure will be designed with accurate control of its geometrical dimensions since the resonant frequency depends on the dimensions. 2) Choosing the right material type

for the resonator. Employing materials with high density and low modulus can help to reduce the resonant frequency and quality factor of the MEMS resonators. 3) Manipulating the medium that surrounds the resonators. Air can be used as a squeeze film damper to dampen the vibration displacement and reduce the quality factor. Compared to the cochlear biomodels which implement fluids, the resonators that operate in air can provide response with better quality factor and sensitivity [5][16]. The design will be presented in Chapter 2 and the mechanical characterisation will be carried out to verify the designed resonant frequency and quality factor of the fabricated MEMS resonators in Chapters 3-4.

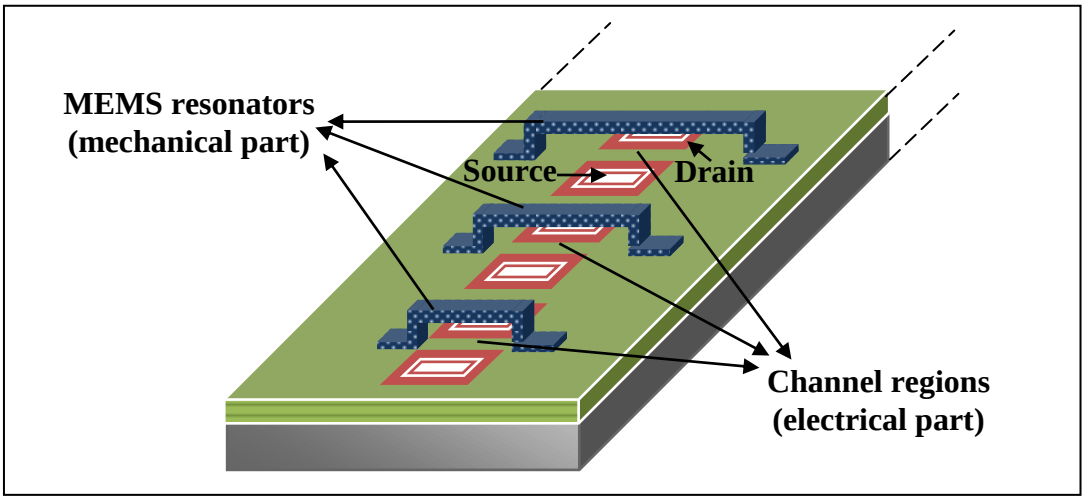


Figure 1.8 *The basic building block for the resonant gate transistor (RGT). The mechanical and electrical parts of RGT are the MEMS resonator bridge structure and the channel region. An array of RGTs is employed in the RGT cochlear biomodel that copies the cochlea's behavioural characteristics.*

1.3.1.2 Channels with source/drain for artificial hair cells

The induced electrical signals from the electrical parts of RGTs possess the same characteristics with those measured from the hair cells. The design and characterisation of the channels and source/drain are crucial in order to ensure that the maximum vibration displacements at resonance of the MEMS resonators could be sensed and transduced electrically at maximum level to the electrical parts of RGTs. The material used for the resonator is required to be conductive in order for the resonator to be able to induce charges within the channel. The fabrication design

for channel and source/drain will be simulated and optimised in Chapter 5. In this work, different channel dimensions and two types of channel i.e. *n*-type and *p*-type will be considered in Chapters 5-7. The electrical characteristics of the channel with and without the air gap spacing between the MEMS resonator and the channel region will be studied and compared. The device's performance will be deduced from the characterisations of the threshold voltage, transconductance and subthreshold current of the channel.

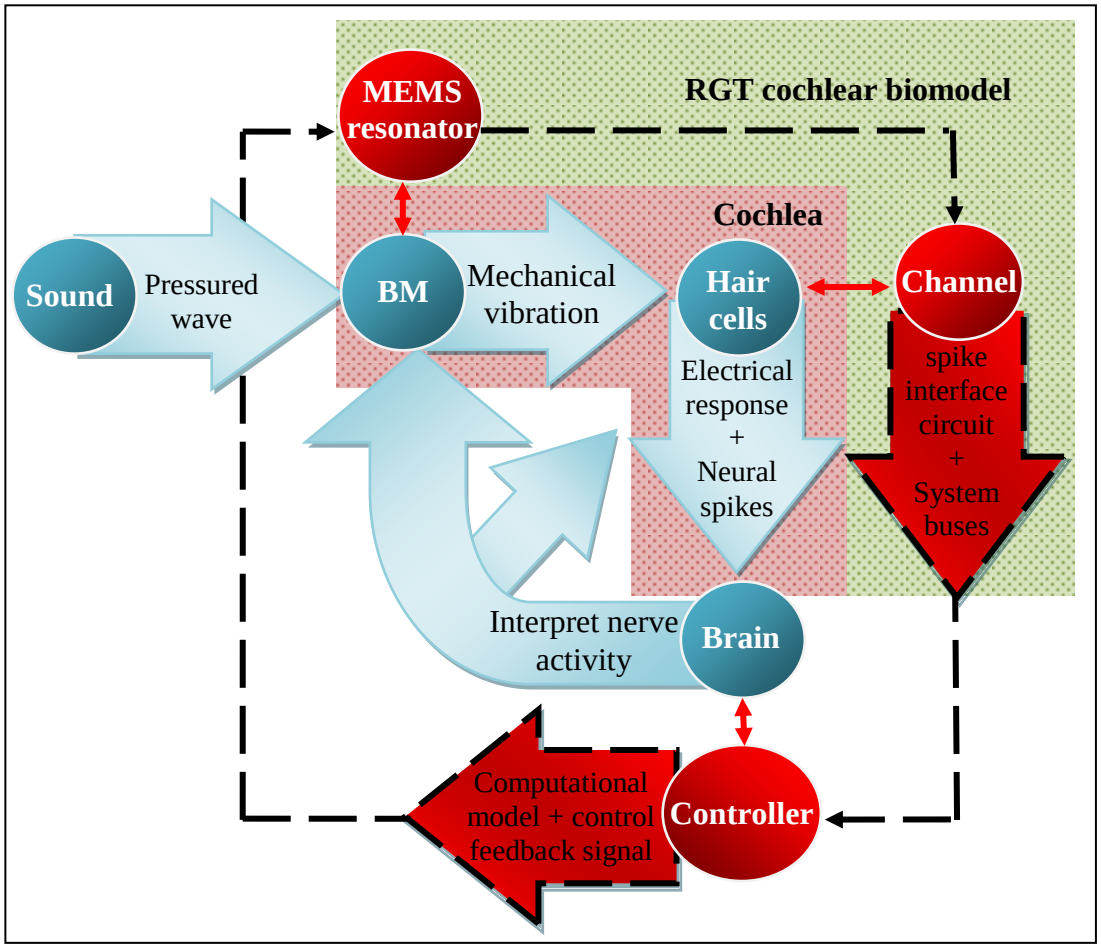


Figure 1.9 *The neuromorphic auditory system copies the process flow of sound analysis by the human auditory system. The RGT cochlear biomodel transduces the sound pressure waves into electrical signals while the controller produces the control signals back to the RGT cochlear biomodel. MEMS resonators and channels within the RGT cochlear biomodel copy the functions of basilar membrane and hair cells within the cochlea.*

1.3.2 Neuromorphic auditory system

The neuromorphic auditory system consists of the RGT cochlear biomodel, neuromorphic circuits, system buses and computational model. In Figure 1.9, the physiological characteristics of the cochlea within the human auditory system are mimicked by the RGT cochlear biomodel within the neuromorphic auditory system. The MEMS resonators and channels of the RGTs represent the basilar membrane and hair cells of the cochlea. The transformation and transmission of neural spikes from the hair cells to brain and the active feedback mechanism from brain to the basilar membrane and/or hair cells can be imitated using the neuromorphic circuits, system buses and the computational model [Figure 1.9].

The electrical signals produced by RGTs can be transformed into spike signals using the spike interface neuromorphic circuits. Then, the transmission of spike signals to the controller can be replicated by employing the system buses on the spike interface neuromorphic circuits. Using the computational model, the controller can process the spike signals and produce the desired control signals back to the MEMS resonator of RGT via the system buses. The adaptive performance of RGT device can be verified by measuring the amplitude and frequency tuning of the mechanical/electrical outputs from RGT device with respect to the control feedback signals. The drive, sense and feedback circuitry will be designed to control the RGT devices individually.

1.3.3 Scope of research

From the human auditory system, the scope of research for this project is limited to the study of the mechanical and electrical characteristics of the cochlea. Thus, the work is focused on the design of RGT devices to copy the mechanical output signals from the basilar membrane and the electrical output signals from the hair cells, physically and mathematically. The neural spike signals from the hair cells are not covered in this study. The neural spike transformation from the mathematical model of RGT will only be discussed briefly in Chapter 2. The outline of the thesis is presented in the next section.

1.4 Thesis overview

An overview of the thesis structure is depicted in Figure 1.10. The thesis is divided into eight chapters. The first two chapters give the general overview of the research and discuss the approach taken for the design of RGTs towards the development of the RGT cochlear biomodel. Then, the study for RGT is divided into two parts, the mechanical and electrical parts. Chapters 3-4 focus on the design and fabrication of the mechanical part of RGT i.e. the MEMS resonator. In Chapter 5, the electrical part of RGT i.e. the channel region with source/drain is designed. Further characterisations on the channel are performed in Chapters 6-7 and finally, the mechanical and electrical parts of the RGT are integrated and measured in these chapters. The performances of the fabricated RGT devices for the application within the RGT cochlear biomodel and some new design considerations to improve the device are discussed in Chapter 8.

A summary of the structure for each chapter in the thesis is presented here:

Chapter 1: Introduction. The anatomy and physiology of cochlea within the human auditory system are reviewed. The fluidic, electronics and MEMS types of cochlear biomodels are reported. The application of MEMS device in cochlear modelling is emphasised in this project. The resonant gate transistors (RGTs) are introduced as the MEMS device for the MEMS cochlear biomodel.

Chapter 2: **Theoretical development and design of resonant gate transistors (RGTs).** The theoretical background of the electromechanical operation for the RGT device is presented. The adaptive spike event coded RGT-cochlear system is proposed. The mathematical model for RGT is developed according to the application of the device in cochlear biomodel. The ouput characteristics from RGT are calculated. *CoventorWare* simulator is used to assist the design of sensitivity and selectivity for MEMS resonators. For channel design, *TSUPREM-4* is used to determine the fabrication parameters in Chapter 5.

Chapter 3: Fabrication process and mechanical characterisation of aluminium bridges. The fabrication process for creating the mechanical part of RGT i.e. the

MEMS resonators is developed in this chapter. The bridge structures are employed as the MEMS resonators. An etch release technique using the downstream oxygen/nitrogen plasma is developed to release the bridges. In the first iteration, the aluminium metal layer is used as the material for the bridge structure. The frequency response and residual stress within the fabricated aluminium bridge are characterised. The induced stress within the aluminium metal causes the bridges of length $> 1\ mm$ to deform and collapse.

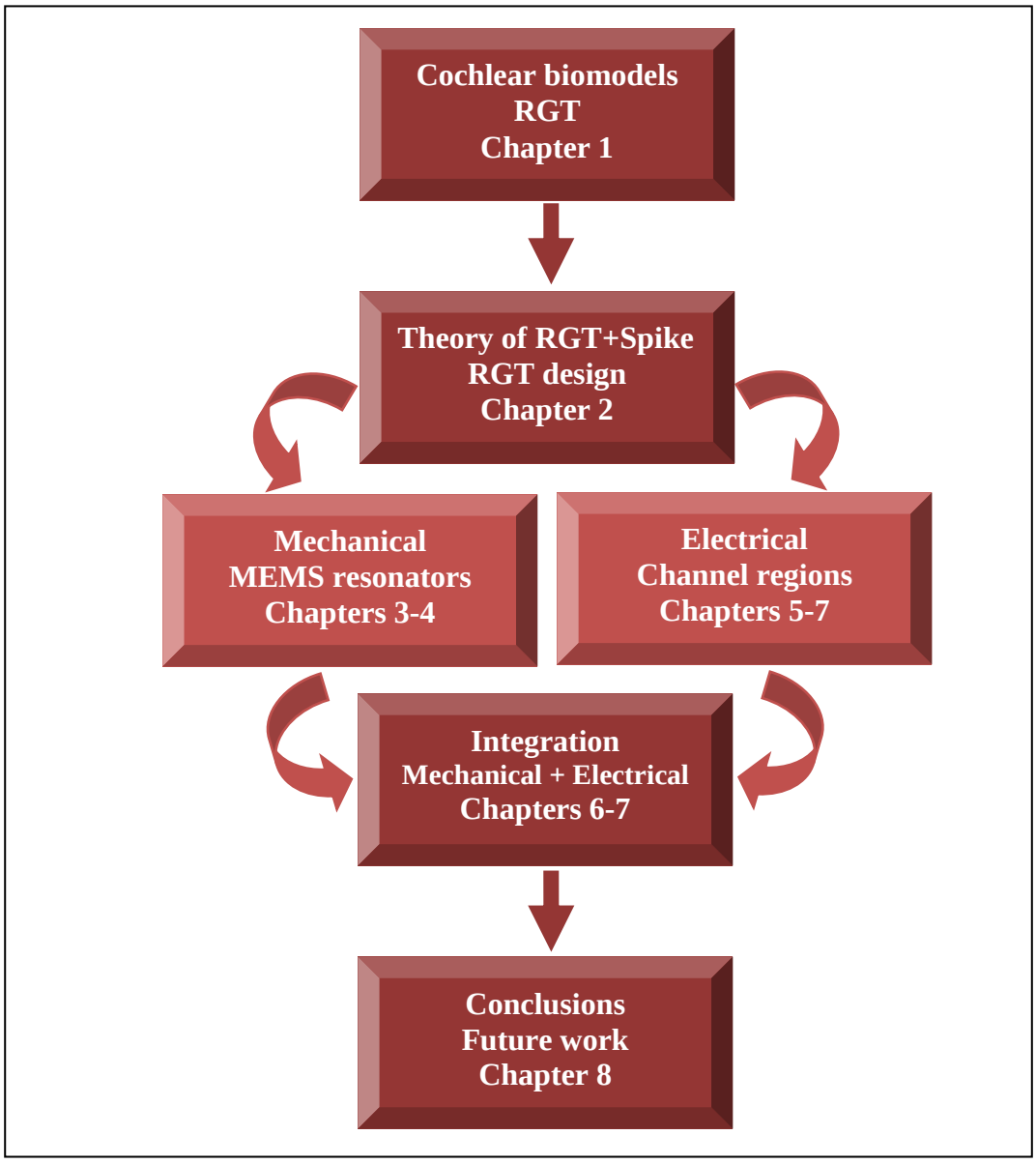


Figure 1.10 *The thesis structure.*

Chapter 4: Fabrication process and mechanical characterisation of tantalum bridges. In the second iteration, the material for the bridge structure is changed from aluminium to tantalum in order to solve the stress issue that has caused the collapsing of the fabricated aluminium bridges with length $> 1\,mm$. Straight and buckled tantalum bridge structures are fabricated and characterised. Even though the residual stress still exists within the bridges, the fabricated structures do not collapse and able to vibrate. The mechanical response and residual stress within the tantalum bridges are studied.

Chapter 5: Design and characterisation of *n*-type channel and source/drain for enhancement and depletion mode *n*-MOSFET. The *n*-channel metal-oxide-semiconductor field-effect transistors (*n*-MOSFETs) are designed and developed in order to investigate the *n*-type channel and source/drain regions of RGT. In the first trial, the enhancement and depletion mode type of *n*-MOSFETs are considered. The fabrication design for the channel and source/drain of *n*-MOSFETs are simulated. For channel, the focus is directed on the design and simulation of the doping profile and threshold voltage. For source/drain, the sheet resistivity of the source/drain regions and the interfacial contact resistivity between source/drain and metal electrode are designed and characterised.

Chapter 6: The measurement and characterisation of *n*-MOSFET and *n*-RGT. In this chapter, the designed enhancement and depletion mode *n*-MOSFET devices from Chapter 5 are fabricated and measured. The threshold voltage, subthreshold current and transconductance of the *n*-MOSFETs are characterised. Then, the *n*-type channel and source/drain regions are integrated with the aluminium or tantalum bridge structure to create the *n*-channel resonant gate transistor (*n*-RGT). The electromechanical behaviours of the fabricated *n*-RGT devices are studied. The measured threshold voltage and transconductance of the *n*-RGTs are compared to those measured from the *n*-MOSFETs. High subthreshold leakage current problem affects the performance of the *n*-channel devices thus, *p*-type channel is pursued next.

Chapter 7: The measurement and characterisation of *p*-MOSFET and *p*-RGT. In the second trial, the *p*-type channel is designed and the enhancement mode *p*-channel metal-oxide-semiconductor field-effect transistors (*p*-MOSFETs) are fabricated. In this chapter, the *p*-type channel and source/drain regions are integrated with the tantalum bridge structure to create the *p*-channel resonant gate transistor (*p*-RGT). The measured threshold voltage and transconductance of the *p*-RGT devices are compared to those measured from the *p*-MOSFETs. The safe operating voltage limit and the electromechanical characteristics of the *p*-RGT devices are characterised. The occurrence of high subthreshold current problem in *n*-channel devices is solved by employing the *p*-channel devices.

Chapter 8: Conclusion. The performances of the fabricated *n*-RGT and *p*-RGT devices for RGT cochlear biomodel are discussed. The recommendations for optimising the device's performance are proposed.

Chapter 2: Theoretical development and design of resonant gate transistors (RGTs)

2.1 Introduction

This chapter describes the theory behind the operation of the resonant gate transistor (RGT) and the application of this device in MEMS cochlear biomodel. The neuromorphic auditory system which integrates the adaptive RGTs with the neuromorphic electronics will be proposed. The mathematical model for RGT will be developed. The MEMS resonator of RGT is modelled using the discrete lumped element model system and the calculated output is compared with the finite element model. Then, the channel of RGT is modelled by including the effect of air gap into the standard transistor equations. The complete simplified mathematical model for RGT device by incorporating the electromechanical equations of MEMS resonator and the modified transistor equations of channel will be described. The created model for RGT will be tested with noise input signals and the corresponding electromechanical response will be estimated. The calculated output from RGT will be fed into the neuromorphic electronics circuit and the generation of spike signals from the chip will be measured.

The developed mathematical model will be used to assist the fabrication design of the RGT device. The geometrical dimensions and the types of material to be used for the MEMS resonator will be decided. The influence of channel dimensions on the electromechanical behaviour of RGT will be discussed. The fabrication design for the channel region will be treated in detail in Chapter 5. Using the designed

parameters, the expected mechanical and electromechanical responses of the RGT devices will be calculated from the developed mathematical model of RGT. The designed parameters for RGT will be optimised in order for the device to mimic the response of a human cochlea.

2.2 The operation of RGT in RGT cochlear biomodel

Nathanson *et al* have first reported on the fabrication of RGT devices that operate within the frequency range of $2.8\,kHz - 60\,kHz$ in 1965 [21][22]. The devices were actuated electrostatically by the AC electrical input signals. In our work, the operation of RGT will be analysed in terms of the mechanical sound pressure waves input signals in order to apply the device within the cochlear biomodel. In Figure 2.1, the sound pressure waves are shown to actuate mechanically the RGT devices in the RGT cochlear biomodel**.** The operation of RGT is described next.

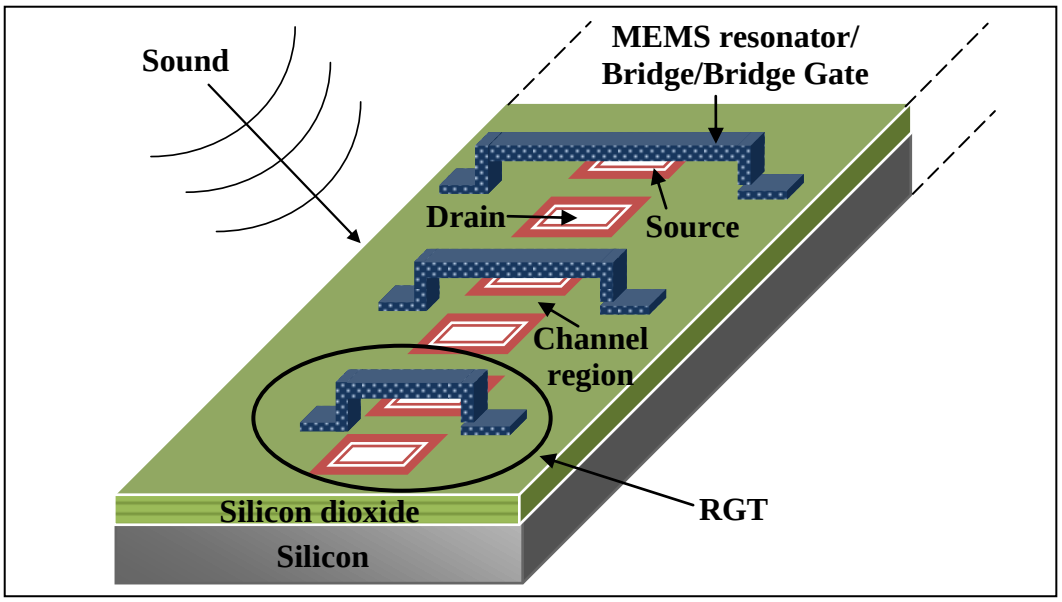


Figure 2.1 *The schematic diagram of RGT cochlear biomodel. An array of RGTs is designed to copy the frequency-to-place mapping characteristics of human cochlea.*

2.2.2 The mechanical sensor

In Chapter 1, the RGT device has been described to be made up of two parts. The mechanical part is the conductive MEMS resonator that acts as a vibration transducer

[Figure 2.1]. The sound pressure wave input signals are sensed directly by the MEMS resonators and transformed into mechanical vibrations. The MEMS resonator vibrates with a certain value of quality factor, resonant frequency and displacement according to the geometrical design of the structure, the properties of the material used and the viscosity of the surrounding medium [21][22]. In this work, fixed-fixed beam structures as shown in Figure 2.1 have been employed as the MEMS resonators and will be now referred to as the bridges.

An array of RGTs with different length of bridges can behave as a real-time frequency analyser, mimicking the functionalities of the basilar membrane in a cochlea. Each bridge of different length will correspond to a different resonant frequency f_1, imitating the frequency-to-place mapping characteristics of the membrane. The bridges are biased with DC voltages in order to transduce the mechanical vibrations into electrical signals within the channels. The sensitivity of the bridge structure could be tuned simply by varying the applied DC bias voltage.

2.2.3 The electrical sensor

The electrical part of RGT device is the channel region with source/drain, located underneath the bridge [Figure 2.1]. The applied DC voltage onto the bridge will induce charges within the channel and modulate the channel conductance. A DC bias is also applied between the source and drain that allows the electrical current signal to flow through the channel. The bridge mechanical vibrations are then transformed into electrical current signal that flows from drain to source. Basically, the bridge structure of RGT acts like a gate for the underneath channel region as in the gate for metal-oxide-semiconductor field-effect transistor (MOSFET) device. Thus, the bridge structure with channel underneath will be referred to as the bridge gate.

Without the channel, the mechanical vibrations of the bridge structure can be detected capacitively. Compared to the capacitive detection method, a channel-based detection technique might propose signal amplification advantage and thus promises higher output capability [23]. It is known that the channel of MOSFET possesses

transconductance which represents gain of the device. The magnitude of transconductance can be designed from the dimensions of the channel region.

2.3 Spike event coded RGT-cochlear system

The neuromorphic auditory system for RGT cochlear biomodel is proposed in Figure 2.2. The adaptive RGT cochlear biomodel is integrated with the spike interface neuromorphic circuit and Address Event Representation protocol (AER) system buses to mimic the transformation and transmission of neural spikes from the hair cells to brain and the active feedback mechanism from brain to cochlea [25].

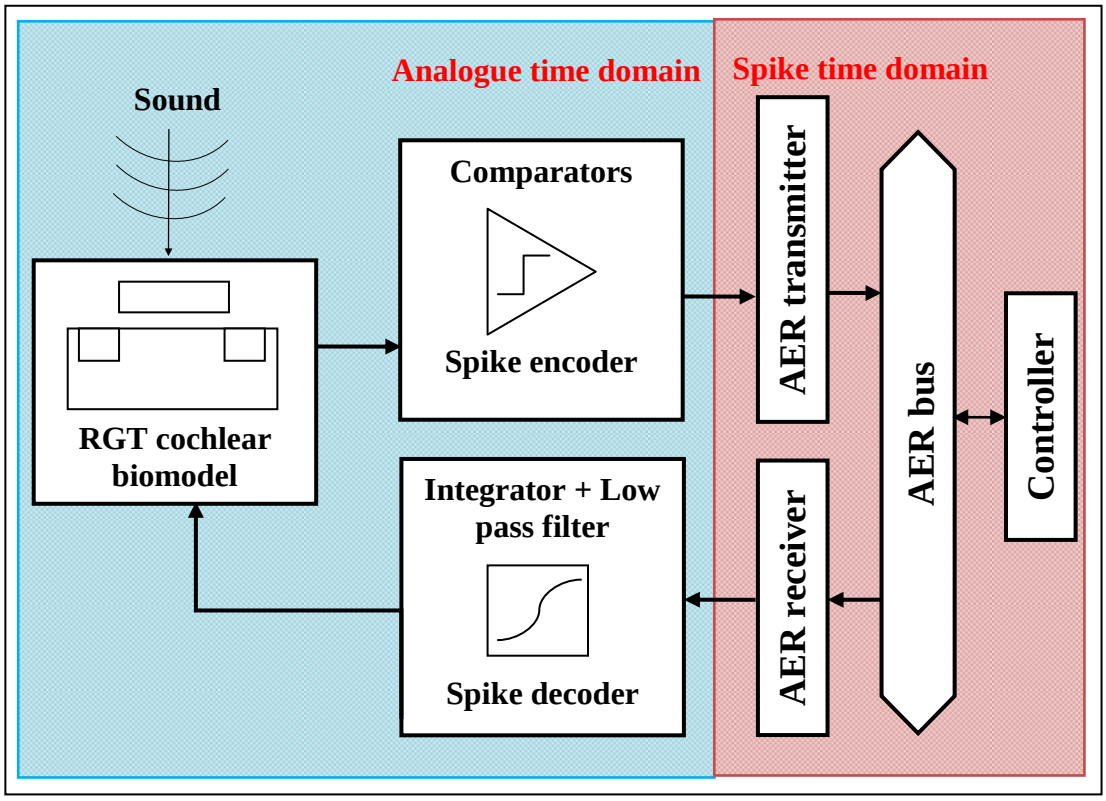


Figure 2.2 *The simplified block diagram of spike event coded RGT-cochlear system for neuromorphic auditory application [25]. The sound input signals are transformed into analogue electrical ouputs by the RGTs. The spike encoder transforms the analogue electrical ouputs into spike time events that are transmitted to the controller via AER protocol. The desired control signals from the controller are transformed into analogue electrical signals by the spike decoder and fed back to the RGTs.*

The proposed neuromorphic auditory system is named as the spike event coded RGT-cochlear system. The sound input signals are sensed directly by the array of RGTs and the analogue current/voltage output signals from the RGTs will be encoded as spike time events by the comparators of the spike time encoder. The spike signals are then transmitted to the external cochlea processor/controller asynchronously using AER protocol interface [25]. The controller processes the received spike signals and generates the desired feedback control signals for RGTs. The feedback control signals in the form of spike representation are first converted into analogue domain by the integrator and low pass filter of the spike event decoder. The analogue time domain control signals are fed back to the RGT cochlear biomodel and the sensitivity and/or selectivity of the RGT devices can be adjusted electrostatically. The prototype for the spike event interface circuit with AER has been fabricated by T. Koickal *et al* [25]. The mathematical model for RGT cochlear biomodel will be created and the calculated responses from the RGTs will be encoded as spike time events by the prototype circuit.

2.4 The mathematical model of RGT

In this section, a simplified mathematical model of RGT has been developed and the ouput characteristics of the device have been estimated. From the model, the expected mechanical and electrical sensitivity of RGT device operating in air have been calculated. Sensitivity is defined as the change in vibration displacement (mechanical sensitivity) or the change in current variation (electrical sensitivity) with respect to the change in sound input pressure applied on the device. The behaviour of RGT device vibrating in vacuum has been described as well. The self-control/tune in the sensitivity and selectivity of the RGT output responses have been calculated. Finally, the encoding of the calculated analogue time domain output signal from the RGT as spike time events have been measured.

2.4.1 Resonant frequency for bridge gate

In order to present the mathematical model of RGT cochlear biomodel, ten RGT devices have been considered. The bridge gates for the RGTs are labelled as $B1$ to

$B10$. The RGTs will be designed to cover the mechanical resonant frequencies, f_1 from $1\ kHz$ to $8\ kHz$. An array of bridge gates that resonates within a certain frequency range can be designed using equation 2.1 where γ is 4.73 for fundamental mode vibration, $A_b = w_b t_b$ is the cross sectional area with w_b and t_b being the width and thickness of the bridge gate, E is the Young's modulus, $I = \frac{w_b {t_b}^3}{12}$ is the moment of inertia, ρ is the density and l_b is the length of the bridge gate structure [30].

$$f_1 = \frac{\gamma^2}{2\pi}\sqrt{\frac{EI}{\rho A_b {l_b}^4}} \tag{2.1}$$

In the mathematical model, aluminium has been considered to be the material for the bridge gate structure, assuming $\rho = 2700\ kgm^{-3}$ and $E = 70\ GPa$. From equation 2.1, in order to achieve $f_1 = 1\ kHz - 8\ kHz$, the length of aluminium bridge gates have been estimated to be $l_b = 1.62\ mm - 0.57\ mm$ with $t_b = 0.5\ \mu m$. The designed tonotopic organisation in RGT array is shown in Table 2.1. The increase of bridge gate length from $B10$ to $B1$ is similar with the increase in basilar membrane width from base to apex. Longer(shorter) aluminium bridge gate represents apex(base) that corresponds to lower(higher) frequency signal.

Label	f_1, kHz	l_b, mm
$B10$	8.0	0.57
$B9$	6.3	0.64
$B8$	5.0	0.72
$B7$	4.0	0.81
$B6$	3.2	0.91
$B5$	2.5	1.02
$B4$	2.0	1.14
$B3$	1.5	1.28
$B2$	1.3	1.44
$B1$	1.0	1.62

Table 2.1 *The estimated aluminium bridge gate length l_b for the resonant frequencies of $f_1 = 1\ kHz - 8\ kHz$. An array of ten RGTs labelled as $B1 - B10$ has been designed to copy the tonotopic organisation in the cochlea.*

2.4.2 Mechanical equivalent lumped element model for bridge gate

The dynamic response of a bridge gate structure could be analysed as the one-degree-of-freedom vibrating system in which the resonating structure is represented by a lumped mass, spring and damper. The general linear second order dynamic equation of the bridge gate is given by d'Alembert's principle in equation 2.2 where F is the net input force that induces sinusoidal deflection on the bridge gate, x is the instantaneous vibration displacement of the bridge gate with respect to time t, m represents the effective bridge gate mass which is approximately 0.767 times its actual mass when force F is distributed over the entire bridge gate, b is the damping coefficient of bridge gate structure and k is the elastic restoring coefficient/the spring constant that quantifies the stiffness of bridge gate [24].

$$m\frac{\partial^2 x}{\partial t^2} + b\frac{\partial x}{\partial t} + kx = F \tag{2.2}$$

From equation 2.2, the amplitude and phase of the bridge gate vibrations are derived into the standard resonance equation in Laplace domain [equation 2.3] where ω_0 is the mechanical resonant radial frequency [equation 2.4], Q_3 is the quality factor at $3\ dB$ below the peak vibration and ζ is the damping ratio of the bridge gate structure [equation 2.5] [24]. $X(s)/F(s)$ is x/F in Laplace domain.

$$\frac{X(s)}{F(s)} = \frac{1}{ms^2 + bs + k} = \frac{1}{k}\left[\frac{1}{1 + \left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q\omega_0}}\right] \tag{2.3}$$

$$\omega_0 = \sqrt{\frac{k}{m}} = 2\pi f_1 \tag{2.4}$$

$$Q_3 = \frac{k}{\omega_0 b} = \frac{1}{2\zeta} \tag{2.5}$$

2.4.2.1 Damping coefficient, b and quality factor, Q_3

From the fabrication process, aluminium bridge gate can be designed to be at a certain distance d_i above the channel. Energy dissipation within the micromachined bridge gate structure is described by several damping mechanisms that depend on d_i

and air pressure conditions [24][26][27]. For a MEMS resonating structure vibrating in standard atmospheric pressure and temperature, the squeeze-film damping will dominate, particularly when the gap size d_i between the structure and substrate is smaller compared to its width and length [24][26][27]. The squeeze film damping b of the bridge gate and the corresponding quality factor approximation Q_3 are given by equation 2.6 and equation 2.7 respectively, with ψ being the viscosity coefficient of the medium surrounding the bridge gate [24]. At a very low pressure for example in vacuum medium, $\psi \to 0$ and the intrinsic material damping of the bridge gate will dominate over the squeeze film damping.

$$b = \frac{3}{2\pi}\frac{\psi(w_b l_b)^2}{{d_i}^3} \tag{2.6}$$

$$Q_3 = \frac{\sqrt{E\rho}{t_b}^2{d_i}^3}{\psi\left(\frac{w_b l_b}{2}\right)^2} \tag{2.7}$$

In our model, the damping of the bridge gate is presented by damping ratio $\zeta = \frac{\omega_0 b}{2k} = \frac{1}{2Q_3}$. The damping ratio is assumed to be $\zeta = 0.01$ in vacuum environment. In air, aluminium bridges have been measured by others to have the squeeze-film damping as much as 10 times bigger than the intrinsic material damping [28]. Thus, the damping ratio is assumed to be $\zeta = 0.1$ for the aluminium bridge gate vibrating in standard atmospheric pressure.

2.4.2.2 Spring constant, *k*

The stiffness of bridge gate for small deflection/vibration cases can be modelled using the linear spring constant, k in equation 2.8 where k' accounts for the bridge gate material properties i.e. Young's modulus and moment of inertia while k'' quantifies the biaxial residual tensile stress induced within the bridge gate during the fabrication process. From the equation of bending, k' is derived in equation 2.9 assuming uniform vertical force F is distributed across the entire bridge gate structure. As for the derivation of k'' in equation 2.10, the bridge gate is modelled as a stretched wire with σ_{tens} being the biaxial residual tensile stress and ν is the

Poisson's ratio of the bridge gate [24]. In the fabrication process, the biaxial residual compressive stress might be induced instead of tensile. The presence of compressive and tensile residual stress within the bridge gate will be treated in detail in Chapters 3-4.

$$k = k' + k" \tag{2.8}$$

$$k' = 32Ew_b\left(\frac{t_b}{l_b}\right)^3 \tag{2.9}$$

$$k" = 8\sigma_{tens}(1-\nu)w_b\left(\frac{t_b}{l_b}\right) \tag{2.10}$$

2.4.3 Mechanical response of bridge gate

The mechanical equivalent lumped element models for the aluminium bridge gates $B1 - B10$ from Table 2.1 have been created using the lumped element parameters m, b, and k. The parameters have been estimated from equation 2.1, equation 2.4, equation 2.5 and equation 2.9. In the model, a constant bridge gate width of $w_b = 10\,\mu m$ has been considered for the bridge gate length of $l_b = 1.62\,mm - 0.57\,mm$. For model simplification, the bridge gates are assumed to be free of stress and the damping ratio is taken as a constant value of $\zeta = 0.1$. At this stage, the total damping is assumed to be constant for all bridge gate lengths. In the fabrication design of RGT in section 2.6.3.1, w_b needs to be varied for each bridge gate length in order to obtain constant damping. The established lumped element model for the aluminium bridge gate $B1$ of length $l_b = 1.62\,mm$ has been tested by applying a uniform load of $0.01\,Pa$. The frequency response of $B1$ has been estimated from the analytical lumped element model and is plotted in Figure 2.3.

In order to verify that the calculated analytical lumped element model for $B1$ is approximately adequate, the numerical finite element (FE) model of the aluminium bridge gate has been simulated using *CoventorWare*. The FE model for $B1$ has been constructed according to its geometrical dimensions and material properties. The steady state linear dynamic response of the constructed FE model for the bridge gate structure has been simulated with respect to the continuous harmonic excitation input

of 0.01 Pa distributed over the entire structure. In the finite element analysis with fixed end boundary condition, the resonant frequencies are computed as the eigenvalues for the undamped, homogenous equation of motion of the structures [29]. In Figure 2.3, the FE simulation result for the aluminium bridge gate $B1$ is compared with the calculated response from the analytical lumped element model. The plot shows an excellent agreement between the two models with the expected resonant frequency of ~1 kHz, maximum displacement of ~1.25 μm and Q_{10}~1.

As the bridge gate length decreases from $B1$ to $B10$, the resonant frequency has been simulated to increase to ~8 kHz while the displacement decreases to ~20 nm. Similarly, the basilar membrane in the cochlea has been measured by others to resonate with smaller amplitude displacements at higher frequencies, in which peak vibration of 20 nm is measured at 1 kHz while 2 nm is measured at 10 kHz [5][6].

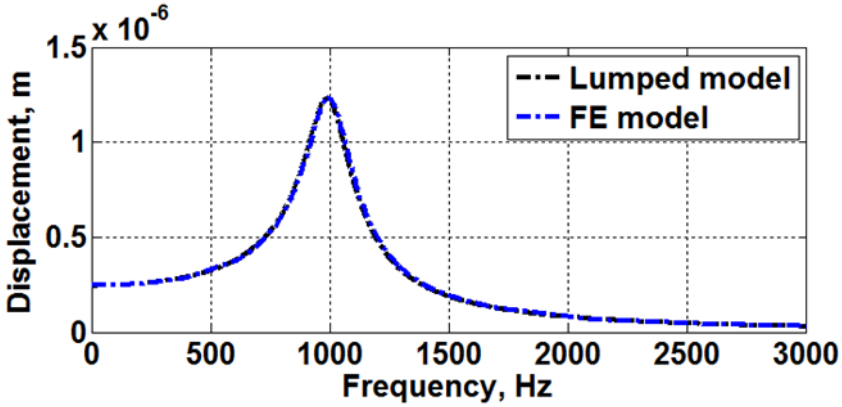
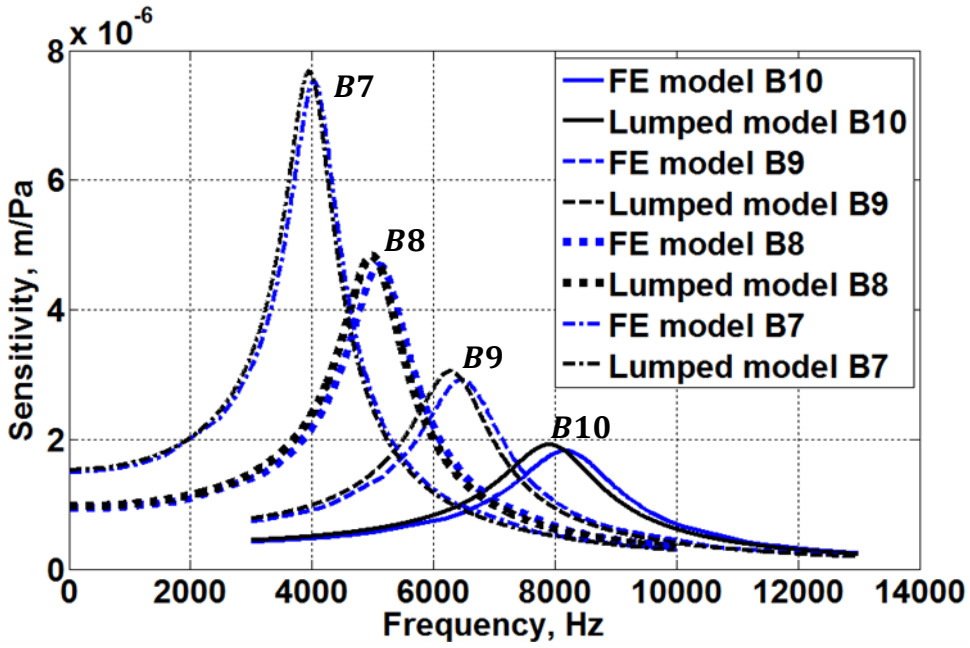


Figure 2.3 *The calculated frequency response from the analytical lumped element model compared to the simulated frequency response from the numerical finite element model of aluminium bridge gate $B1$ with $l_b = 1.62\ mm$.*

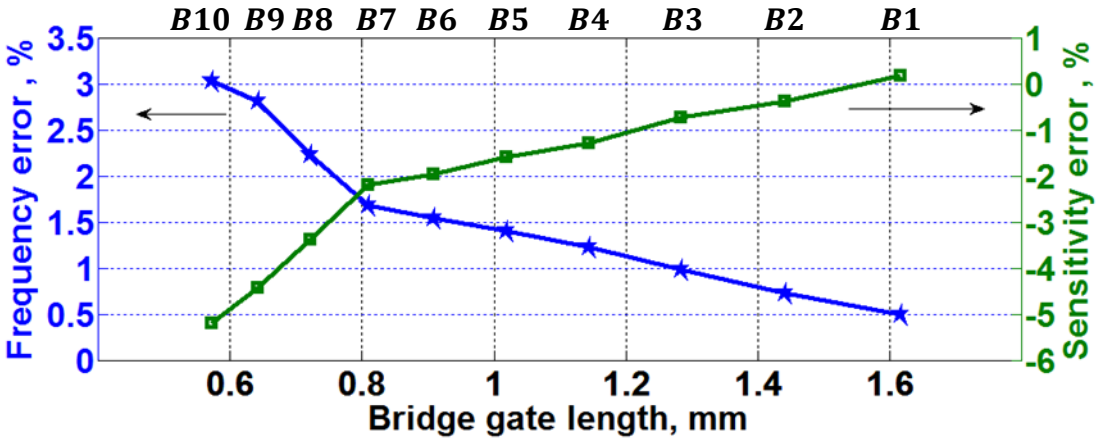
2.4.3.1 Lumped element model error

In this section, an increase of disagreement between the analytical lumped element model and numerical FE model has been observed as the bridge gate length decreases. The percentage differences between FE and lumped element model have been computed from the mechanical sensitivity and frequency of the aluminium bridge gates $B1 - B10$. The FE simulation results and lumped element model

calculations for $B7 - B10$ of $l_b = 0.81\,mm - 0.57\,mm$ are plotted together in Figure 2.4(a) showing the increase of discrepancies between the two models as the bridge gate length decreases from $B7$ to $B10$.



(a) Frequency responses for $B7 - B10$



(b) FE and lumped element model percentage errors for $B1 - B10$

Figure 2.4 *(a) The comparison of frequency responses between FE model and lumped element model for aluminium bridge gate* $B7 - B10$ *of length* $l_b = 0.81\,mm - 0.57\,mm$. *(b) The increase of frequency and mechanical sensitivity percentage errors between the FE and lumped element models as the bridge gate length decreases from* $B1$ $(l_b = 1.62\,mm)$ *to* 10 $(l_b = 0.57\,mm)$.

The resonant frequency from the FE model has been simulated to be higher than lumped element model while the mechanical sensitivity is becoming smaller. Figure 2.4(b) shows the frequency and sensitivity percentage difference between the two models for $B1$ to $B10$ i.e. $l_b = 1.62\ mm$ to $0.57\ mm$. For $B1$ to $B6$ of $l_b = 1.62\ mm - 0.91\ mm$, the models agree well with each other, with the percentage errors for both frequency and sensitivity being less than 2%. As the bridge gate length continues to decrease from $B7$ to $B10$, the percentage error of the analytical lumped element model from FE model for both frequency and sensitivity have been calculated to increase.

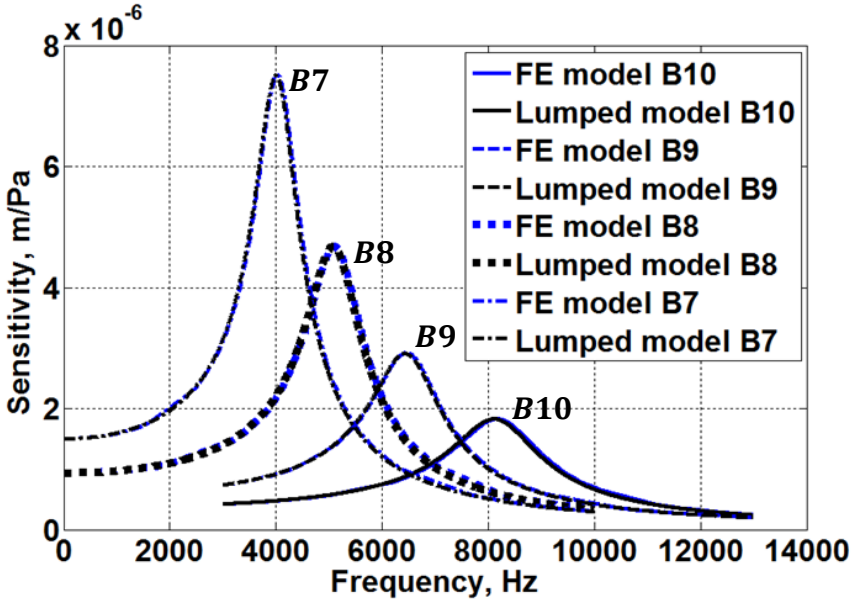
The positive(negative) percentage value indicates the resonant frequency or sensitivity of the FE model being higher(smaller) than lumped element model. The discrepancies in frequency responses between the two models might be due to the limitation of the analytical bridge gate theory, leading to inaccurate estimation of m, b and k for the lumped element model.

2.4.3.2 Lumped element model correction

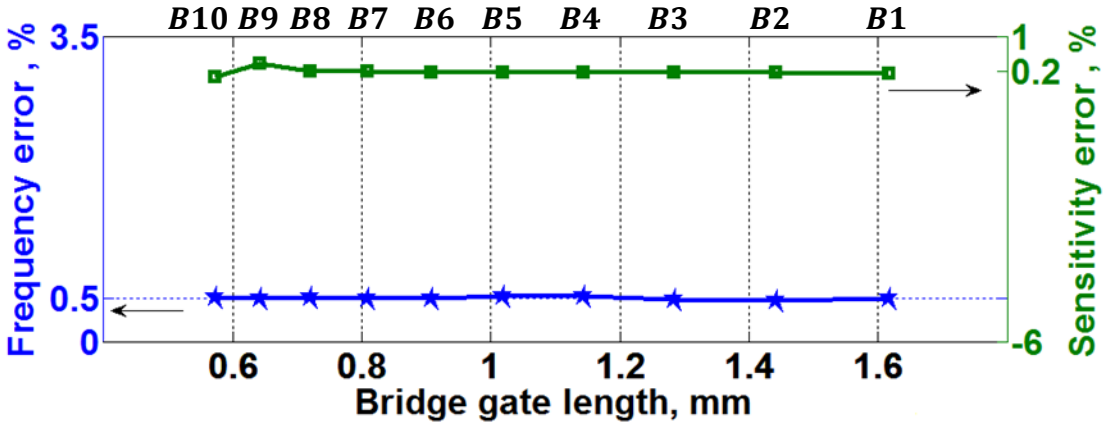
In order to obtain a more accurate response of the bridge gate from the lumped element model, the approximate values of b and k parameters for the model can be extracted from the simulated response of the bridge gate in FE model. Thus, the lumped element model has been reconstructed using the estimated b and k from FE model plus the effective mass m of the bridge gate structure. The frequency responses from the reconstructed lumped element models have been calculated and fitted to the FE simulation results in Figure 2.5(a) with small frequency and mechanical sensitivity percentage errors in Figure 2.5(b).

In future, different shapes of MEMS resonator other than the simple form of bridge structure could be employed for better RGT cochlear biomodel application, for instance the crab-legged or serpentine features described in Chapter 8. A complex theory and analysis will be required to design these complicated structures. In addition, advanced analysis is necessary in order to incorporate damping according

to the structure's geometry and/or to account for the presence of different stress type, either compressive or tensile within the structures. Thus, FE model simulation in *CoventorWare* can assist the analysis of the structure and better lumped element model can be developed from the corresponding FE model.



(a) Frequency responses for $B7 - B10$

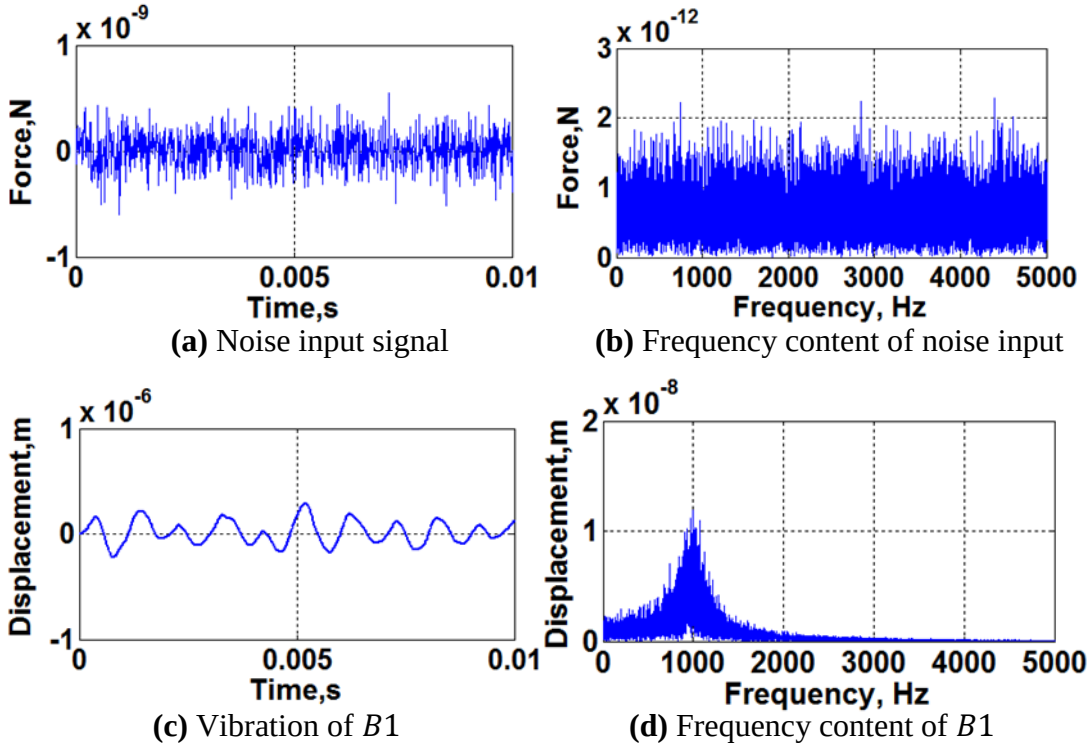


(b) FE and lumped element model percentage errors for $B1 - B10$

Figure 2.5 *The lumped element model has been reconstructed to fit the FE model. (a) The fitting of frequency responses from the reconstructed lumped element model to FE model for the aluminium bridge gates* $B7 - B10$ *of length* $l_b = 0.81\ mm - 0.57\ mm$. *(b) Small frequency and mechanical sensitivity percentage errors between the reconstructed lumped element and FE models as the bridge gate length decreases from* $B1$ $(l_b = 1.62\ mm)$ *to* 10 $(l_b = 0.57\ mm)$.

2.4.3.3 Lumped element model testing

Next, the reconstructed analytical lumped element model for $B1$ has been tested with 0.01 Pa of noise input signal which represents the mechanical force F in equation 2.2. The noise input signal in analogue time domain is shown in Figure 2.6(a) and the corresponding spectral domain representation of the input signal is plotted in Figure 2.6(b). The calculated mechanical response from the model is shown in Figure 2.6(c)-(d). $B1$ resonates at the designed frequency $f_1 \sim 1\ kHz$ and filters all other frequencies outside of the designed value. In the following section, the instantaneous vibration displacements of the bridge gate with respect to time, $x(t)$ in Figure 2.6(c) will be transduced into the electrical signals within the channel region.



(a) Noise input signal **(b)** Frequency content of noise input

(c) Vibration of $B1$ **(d)** Frequency content of $B1$

Figure 2.6 *(a)-(b) The noise input signal in time and frequency domains. (c)-(d) The calculated mechanical response of $B1$ in time and frequency domains with respect to the applied noise input.*

2.4.4 Electromechanical model of RGT

From Figure 2.1, the cross sectional view of RGT device is shown in Figure 2.7. From the fabrication process, the bridge gate can be designed to be at certain distance

d_i above the channel region. Basically, the channel region consists of 1) the channel inversion layer within the silicon substrate and 2) the grown silicon dioxide layer as the gate oxide [Figure 2.7]. The DC voltage V_{gs} is applied onto the bridge gate structure to modulate the channel conductance and V_{ds} is applied to induce the electrical current I_{ds} to flow from drain to source. The bridge gate instantaneous vibration $x(t)$ at the constant voltage V_{gs} will vary the modulation of channel conductance and thus vary the drain current I_{ds} with respect to time.

In this section, the analytical electromechanical response of RGT device that employs bridge gate $B7$ of length $l_b = 0.81\ mm$ has been investigated. From Figure 2.5 and Table 2.1, the expected resonant frequency for the RGT device of $l_b = 0.81\ mm$ is $f_1 = 4\ kHz$. The lumped element model has been created for bridge gate $B7$ and the corresponding mechanical response $x(t)$ has been calculated. The tuning characteristics for the bridge gate $B7$ with respect to the applied V_{gs} will be demonstrated in section 2.4.4.2. Using $x(t)$, the small signal drain current $I_{ds}(t)$ of the RGT device will be calculated in section 2.4.4.4.

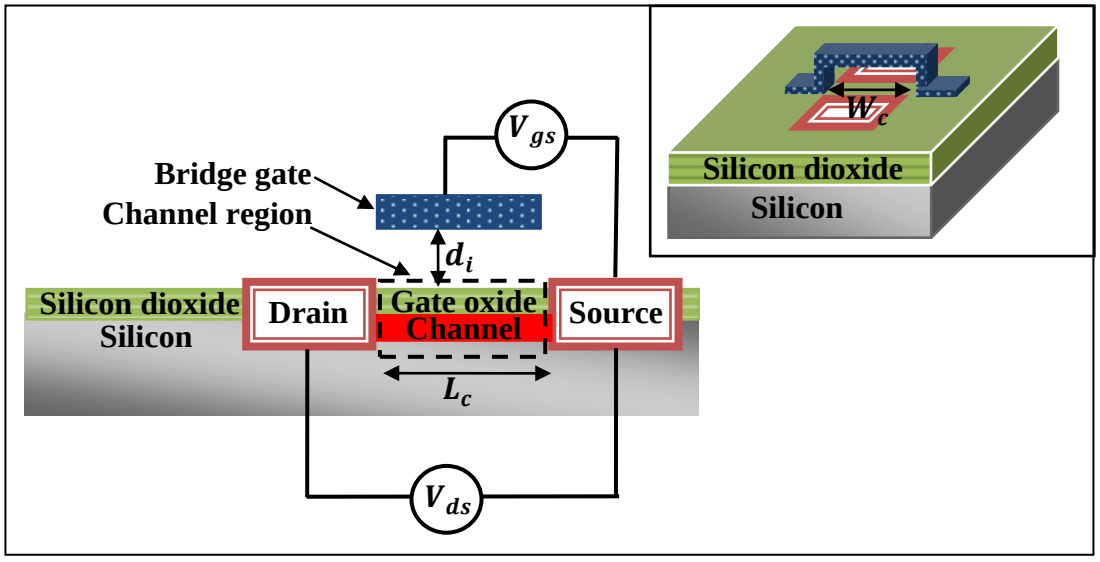


Figure 2.7 *The cross sectional view of RGT device which is biased with V_{gs} and V_{ds} in order to induce current flow through the channel. d_i denotes the air gap distance from the channel region to bridge gate while L_c defines the channel length. In the subset, W_c defines the channel width.*

2.4.4.1 Limit of V_{gs} for RGT

Before calculating the electrical current output and the tuning characteristics of RGT, the minimum and maximum values of V_{gs} that should be applied onto the bridge gate have to be defined. In order for the modulation of channel conductance to occur, the minimum DC bias applied onto the bridge gate needs to be higher than the threshold voltage V_{th} of the channel. V_{th} depends on the air gap distance d_i from the bridge gate to channel region, metal-silicon work function $\breve{\varphi}_{MS}$ from the bridge gate to channel, properties of the silicon dioxide gate oxide layer and channel doping within the silicon substrate. The fabrication design for the channel region and the effect of d_i on V_{th} will be described in Chapters 5-7.

Due to the applied V_{gs}, an attractive electrostatic force F_e is exerted between the bridge gate and channel. F_e will be counterbalanced by the mechanical restoration force F_m that appears due to the elasticity of the bridge gate structure. Consequently, the equilibrium distance of the bridge gate from channel is reduced [21]. The pull-in voltage, V_{pi} is the maximum voltage that could be applied onto the bridge gate before F_m is unable to maintain the equilibrium state due to the increase of F_e and causes the structure to snap/collapse onto the channel region.

$$V_{pi} = \sqrt{\frac{8k{d_i}^3}{27\varepsilon_0 A_c}} \tag{2.11}$$

The pull-in voltage is defined in equation 2.11 where A_c is the area of channel region and ε_0 is the permittivity of air [21]. From Figure 2.7, the channel area is defined as $A_c = W_c \times L_c$ with W_c and L_c being the width and length of the channel. L_c also represents the width of the bridge gate, w_b. From equation 2.9, $k \propto \frac{1}{{l_b}^3}$. Thus, the pull-in voltage for $B1 - B10$ bridge gate structures will increase with respect to the decrease of l_b assuming t_b, w_b, E, d_i and A_c to be constant for each bridge gate.

$$V_{th} < V_{gs} < V_{pi} \tag{2.12}$$

The regime of operation for V_{gs} is defined in equation 2.12. The pull-in voltage sets the maximum limit of the safe operating voltage or feedback control voltage that can

be applied onto the bridge gate. The threshold voltage sets the minimum limit of V_{gs} to be applied in order for the channel conductance to modulate.

2.4.4.2 Electromechanical tuning characteristics of RGT

As the applied V_{gs} increases, there are 2 electromechanical effects to be expected to happen on the bridge gate structure. 1) The attractive electrostatic force F_e between the bridge gate and channel increases. Thus, within the regime of operation for V_{gs}, the bridge gate undergoes a small deflection and the air gap distance reduces from d_i to d_n without snapping onto the channel region as the applied V_{gs} increases. The relationship between the change in air gap spacing distance $(d_i - d_n)$ and the applied voltage onto the bridge gate V_{gs} is given by equation 2.13. 2) The interaction between electrostatic force F_e and mechanical restoring force F_m within the bridge gate causes the elastic restoring coefficient k to vary. In equation 2.14, k reduces to k_n with respect to the increase of V_{gs}. Consequently, the resonant frequency of the bridge gate is reduced from its designed mechanical resonant radial frequency of ω_o to ω_n as indicated in equation 2.15.

$$V_{gs} = \sqrt{\frac{2k(d_i - d_n){d_n}^2}{\varepsilon_0 A_c}} \tag{2.13}$$

$$k_n = k - \frac{\varepsilon_0 A_c {V_{gs}}^2}{{d_n}^3} \tag{2.14}$$

$$\frac{\omega_n}{\omega_o} = \sqrt{\frac{k_n/m}{k/m}} \tag{2.15}$$

From the lumped element model, the mechanical response of $B7$ without the influence of V_{gs} has been calculated and labelled as V_{gs0} in Figure 2.8. The resonant frequency at V_{gs0} has been estimated to be $f_1 = 4\ kHz$. The applied V_{gs} has been increased and the corresponding lumped element models based on the changes of k have been calculated. In our model, the tuning behaviour of the RGT device is calculated for $V_{gs1} = \frac{5V_{pi}}{10}$, $V_{gs2} = \frac{8V_{pi}}{10}$ and $V_{gs3} = \frac{9V_{pi}}{10}$, respectively. The tuning

characteristics of $B7$ due to the applied voltages of $V_{gs1} < V_{gs2} < V_{gs3}$ are plotted in Figure 2.8. As the applied voltage onto the bridge gate increases, the resonant frequency has shifted to values smaller than 4 kHz and the increase of gain has been observed.

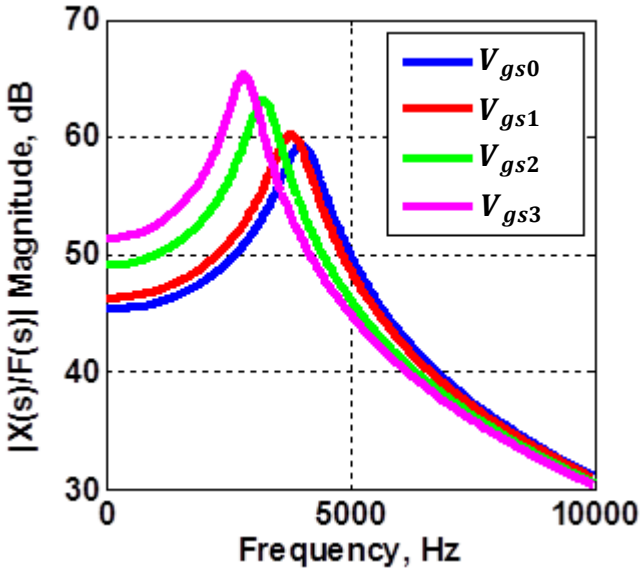


Figure 2.8 *The analytical lumped element models of $B7$ at different values of V_{gs} applied onto the bridge gate. At 0 V, $V_{gs} = V_{gs0}$ and then the applied voltage increases from V_{gs1} to V_{gs3}. The gain and resonant frequency of the bridge gate have been tuned electrostatically with respect to V_{gs}.*

With the increase of V_{gs0} to V_{gs3}, the resonant frequency decreases to 28 % from 4 kHz while the gain becomes ~2 times greater than the gain of the bridge gate at V_{gs0}. Thus, the amplitude of bridge gate vibration can be amplified or attenuated electrostatically by the applied DC voltage and at the same time, the tuning of resonant frequency can also be achieved.

2.4.4.3 Capacitance model of RGT

In RGT, the part from the bridge gate to channel can be modelled as a parallel plate capacitor. The total capacitance between the bridge gate and channel per unit area C_{total} has been taken as the series capacitance of air C_{air} and gate oxide C_{ox} shown in equation 2.16 to equation 2.18 with ε_{ox} and t_{ox} being the permittivity and

thickness of the silicon dioxide gate oxide layer. The DC biased bridge gate vibration $x(t)$ induces capacitance variation with respect to time. Since $t_{ox} \ll d_n$, $C_{ox} \gg C_{air}(t)$ giving $C_{total}(\mathrm{t}) \approx C_{air}(t)$.

$$C_{air}(t) = \frac{\varepsilon_0}{d_n \mp x(t)} \tag{2.16}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.17}$$

$$C_{total}(t) = C_{air}(t) \parallel C_{ox} = \frac{\varepsilon_0}{d_n \mp x(t) + \frac{\varepsilon_0}{\varepsilon_{ox}} t_{ox}} \tag{2.18}$$

When the bridge gate experiences the electromechanical deflection, the air gap spacing is actually a function of position along the bridge gate. In this work, the analysis is simplified by assuming the effective value of air gap spacing distance d_n between the bridge gate and channel region to be independent of position.

2.4.4.4 Drain current I_{ds} response of RGT

The variation in total capacitance with respect to time $C_{total}(t)$ which is triggered by the vibration of bridge gate $x(t)$ held at a constant voltage V_{gs} is comparable to the operation of the metal-oxide-semiconductor field-effect transistor (MOSFET) device in which the gate is fixed in position but the voltage applied onto the gate changes with respect to time $V_{gs}(t)$ [21]. The drain current model for a MOSFET has been modified by including the effect of air gap spacing and electromechanical characteristics of the bridge gate described in $C_{total}(t)$. Thus, the drain current model for RGT in saturation regime is derived in equation 2.19 with μ being the mobility of the charge carriers within the channel. The static drain current model for RGT device and the threshold voltage of the channel will be described further in Chapter 7.

Overall, V_{gs} can control both the magnitude of the bridge gate displacement $x(t)$ and the induced charges within the channel. Increasing the applied V_{gs} onto the bridge gate has been described in the previous section to reduce k and thus increases $x(t)$.

At the same time, d_i is reduced to d_n giving higher $C_{total}(t)$ and smaller threshold voltage V_{th}. The total increment of $x(t)$, $C_{total}(t)$ and V_{gs} plus the reduction of V_{th} will be expected to increase $I_{ds}(t)$.

$$I_{ds}(t) = \frac{\mu C_{total}(t)}{2}\frac{W_c}{L_c}\left(V_{gs} - V_{th}\right)^2 \tag{2.19}$$

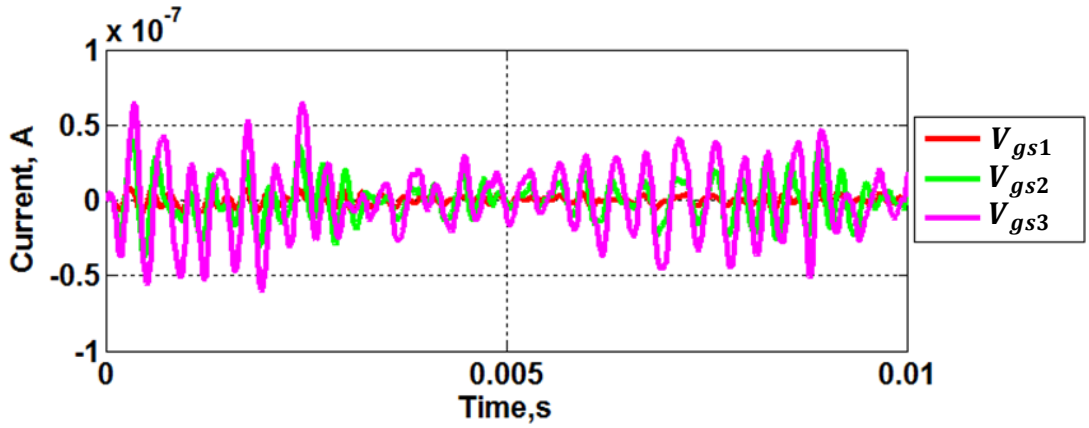
The transconductance g_m can be used to represent gain of the RGT device which quantifies the transduction of the bridge gate vibration $x(t)$ biased at a constant voltage V_{gs} into small signal drain current output $I_{ds}(t)$. By changing the role of the vibrating bridge gate structure at a constant voltage V_{gs} with the equivalent change in voltage $V_{gs}(t)$ applied on a fixed non-vibrating bridge gate, the transconductance g_m is defined in equation 2.20. In Chapters 6-7, the transconductance of the fabricated RGT devices will be characterised.

$$g_m = \frac{\partial I_{ds}(t)}{\partial V_{gs}(t)} = \mu C_{total}\frac{W_c}{L_c}\left(V_{gs} - V_{th}\right) \tag{2.20}$$

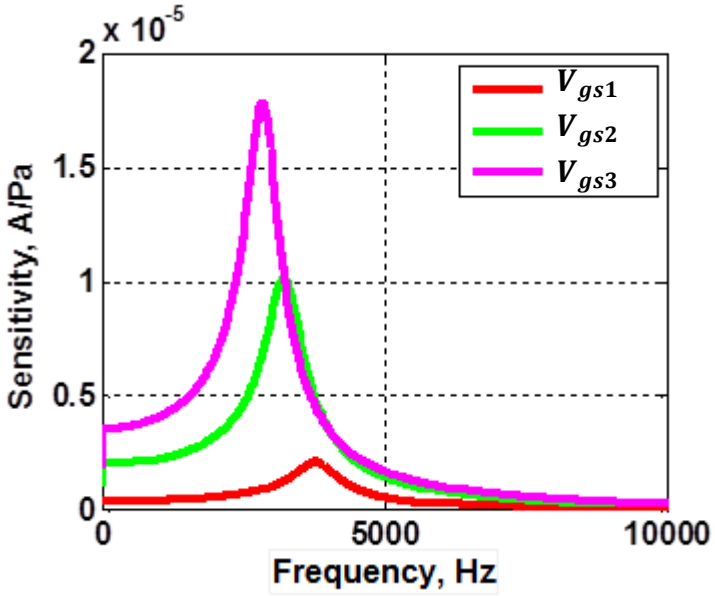
The channel region can be designed to be positioned underneath the antinode of the fundamental bridge gate vibration. At this position, the vibration displacement is at maximum level. Thus, maximal transduction from the mechanical structure to the channel region can be achieved. In addition, the transconductance value g_m can be designed by manipulating the geometrical dimensions of the channel region. From equation 2.20, $\frac{W_c}{L_c}$ ratio can be increased in order to obtain higher g_m. The drain current model for RGT with bridge gate $B7$ of length $l_b = 0.81\,mm$ has been created and tested with $0.01\,Pa$ of noise input signal. The values of $W_c = 80\,\mu m$, $L_c = 10\,\mu m$, $t_{\mathrm{ox}} = 55\,nm$ and $\mu = 1400\,cm^2/Vs$ have been assumed in the model.

The bridge gate voltage of $V_{gs1} = \frac{5V_{pi}}{10}$ has been considered and increased to $V_{gs2} = \frac{8V_{pi}}{10}$ and $V_{gs3} = \frac{9V_{pi}}{10}$. The applied bridge gate voltages are within the regime of operation for V_{gs} i.e. $V_{th} < V_{gs} < V_{pi}$ with the threshold voltage for $B7$ assumed to be $V_{th} = \frac{V_{pi}}{10}$. The RGT device operates within the saturation regime and the calculated electrical output drain current $I_{ds}(t)$ from the device at $V_{gs1} < V_{gs2} < V_{gs3}$ have

been plotted in Figure 2.9(a). The amplitude of drain current in time domain has been seen to be amplified when the applied voltage onto the bridge gate increases.



(a) I_{ds} in time domain



(b) Sensitivity of I_{ds} in frequency domain

Figure 2.9 *The calculated drain current response of RGT with B7 of $l_b = 0.81\ mm$ at $V_{gs1} < V_{gs2} < V_{gs3}$ (a) in time domain and (b) in frequency domain. The gain and resonant frequency of RGT have been tuned electrostatically with respect to V_{gs}.*

In Figure 2.9(b), the calculated electrical sensitivities of RGT in spectral domain at $V_{gs1} < V_{gs2} < V_{gs3}$ are shown. The expected output currents at resonance for $1\ Pa$ of input signal have been calculated to increase from $\sim 2\ \mu A$ to $18\ \mu A$ with respect to

the increase of V_{gs}. As the applied V_{gs1} increases to V_{gs3}, the gain of RGT increases to almost 8.5 times greater than the gain calculated at V_{gs1}, and the resonant frequency has decreased to 25 %. The tuning characteristics of I_{ds} at different values of V_{gs} have been observed to follow the electromechanical tuning characteristics of the bridge gate structure $B7$ from Figure 2.8. This is similar to the electrical frequency response of one hair cell that has been reported to follow closely the mechanical frequency response of a section point in the basilar membrane [5][6].

2.5 Spike coding of RGT output

The drain current model has been created for RGT with bridge gate $B3$ of length $l_b = 1.28\,mm$ giving $f_1 = 1.5\,kHz$. The calculated current output from RGT in analogue time domain $I_{ds}(t)$ has been converted into voltage $V_{out}(t)$. Then, the voltage signal has been coded into spikes using the fabricated spike event encoder prototype chip. The measured spike signals in spike time domain from $V_{out}(t)$ are shown in Figure 2.10. The spike event ouputs are presented in positive or negative pulses. Positive spike events (PSPK) have been generated as the instantaneous $V_{out}(t)$ signal goes up while negative spike events (NSPK) have been generated when the direction of $V_{out}(t)$ signal goes down.

The spikes are generated asynchronously depending on the activity of RGT output signal, $V_{out}(t)$. The magnitude of $V_{out}(t)$ is given by $|V_{out}(t)|$. The spike interval is an inverse function of $|V_{out}(t)|$ derivative [25]. Thus, the spike interval decreases as the rate of change for $|V_{out}(t)|$ increases. This means that higher numbers of spikes are generated to represent the rapid change in magnitude of RGT signal. On the other hand, the spike interval increases when the rate of change for $|V_{out}(t)|$ decreases, generating smaller numbers of spikes. No spikes are generated for a constant signal from RGT or if the rates of magnitude change are below the threshold value. Overall, the created mathematical model for RGT and the measured results from the spike encoder chip have been shown to mimic the functions of basilar

membrane and hair cells in the cochlea that transduce the mechanical sound input signals into neural spike signals.

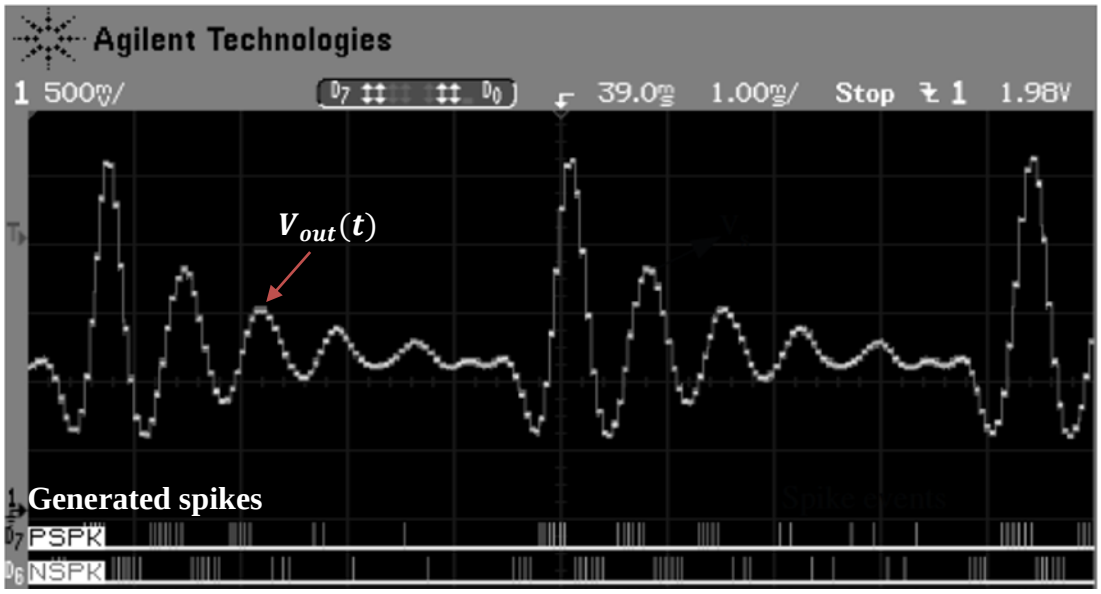


Figure 2.10 *The generation of spikes from the calculated RGT voltage output $V_{out}(t)$. The measured spike event outputs are shown as two separate signals, PSPK and NSPK which represent the direction of RGT signal, either going up or down. Higher numbers of spikes are generated for higher rate of change in magnitude of $V_{out}(t)$ and vice versa.*

2.6 Bridge gate fabrication design and channel dimension consideration for RGT cochlear biomodel

In this section, the designed layout for the fabrication of RGTs on a chip of 1 $cm \times$ 1 cm size will be presented. Due to the limitation in fabrication, the minimum width that can be patterned and fabricated practically for the bridge gate structure is $w_b = 2\ \mu m$. The limits in geometrical dimensions, the selections of bridge gate structural forms and the available materials that can be employed to fabricate the bridge gate will be discussed.

The established mathematical model for RGT will be used for designing and estimating the outputs from the RGT devices. The influence of channel width W_c on the pull-in voltage V_{pi} will be discussed. The designed parameters for RGT are

optimised in order for the device to mimic the response of a human cochlea and to make sure that the designed parameters are feasible for fabrication. For the fabrication design of the channel region and source/drain, *TSUPREM-4* will be used to determine the fabrication parameters in Chapter 5.

2.6.1 MEMS resonator structural shape design

From the mathematical model of RGT, the bridge shape has been chosen as the resonating structure for RGT due to the simplicity of its design and analysis compared to other complex MEMS resonator shapes like crab-legged or serpentine [Figure 2.11][24]. In addition, the bridge structure is more stable compared to cantilever due to the dual supports from its two anchors. From the fabrication point of view, the bridge can be fabricated with small and controllable gap spacing between the bridge and substrate [18].

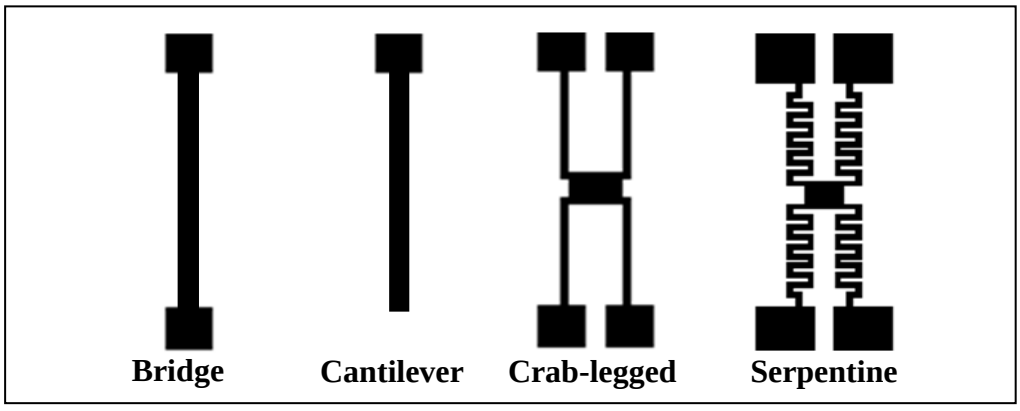


Figure 2.11 *Top views for different shapes of MEMS resonating structures that can be employed in RGT cochlear biomodel. The design of bridge is simpler compared to the crab-legged or serpentine and more stable compared to the cantilever.*

2.6.2 Material and geometry design for resonant frequency f_1

From the mathematical model of RGT described in sections 2.4.1 and 2.4.2, three factors have been considered in order to design the mechanical bridge gate structures to mimic the cochlear response. The first two factors are the geometrical dimensions and the properties of material used for the structures. Simplifying equation 2.1 into equation 2.21, the resonant frequency f_1 of a bridge gate structure can be designed to

operate within the audible frequency range by manipulating its length and thickness; and by choosing the appropriate values of Young's modulus and density of the material structure. From equation 2.21, relatively long and thin bridges with small $\frac{E}{\rho}$ ratio are desired in order to cover the audible frequency range signals.

$$f_1 = 1.028 \frac{t_b}{{l_b}^2} \sqrt{\frac{E}{\rho}} \tag{2.21}$$

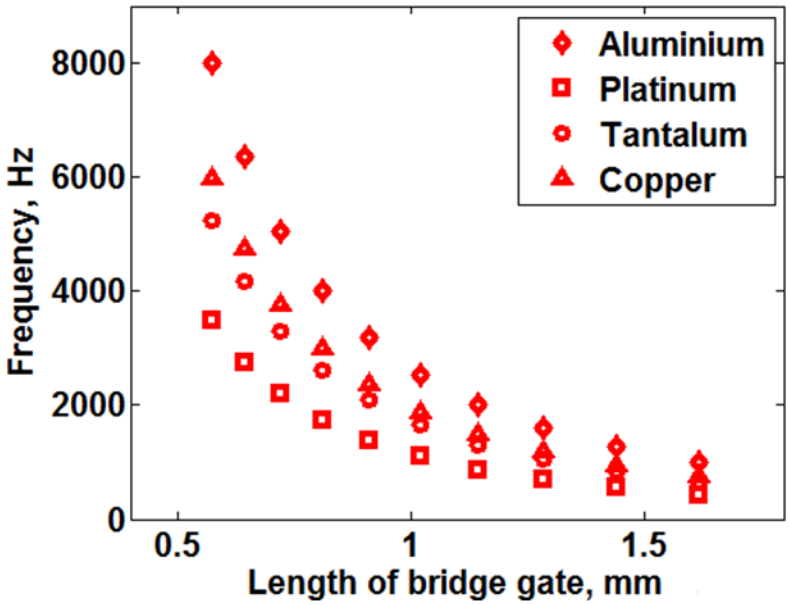


Figure 2.12 *The calculated resonant frequencies for platinum, tantalum, copper and aluminium bridge gates of length* $l_b = 1.62\ mm - 0.57\ mm$ *and thickness* $t_b = 0.5\ \mu m$. *The increase of* $\frac{E}{\rho}$ *ratio from platinum* (5), *tantalum* (11), *copper* (14) *to aluminium* (26) *will increase the resonant frequency of the bridge gate structure.*

2.6.2.1 Influence of E/ρ ratio on resonant frequency f_1

The available materials with small $\frac{E}{\rho}$ ratio which can be used to fabricate the bridge gate structures are aluminium ($\frac{E}{\rho} \approx 26\ \frac{MPa}{kgm^{-3}}$), tantalum ($\frac{E}{\rho} \approx 11\ \frac{MPa}{kgm^{-3}}$), platinum ($\frac{E}{\rho} \approx 5\ \frac{MPa}{kgm^{-3}}$) and copper ($\frac{E}{\rho} \approx 14\ \frac{MPa}{kgm^{-3}}$), assuming bulk values of E and ρ for the metals. In section 2.4.1, an array of ten aluminium bridge gate structures have

been considered with length $l_b = 1.62\ mm - 0.57\ mm$ and thickness $t_b = 0.5\ \mu m$. In Figure 2.12, the resonant frequencies f_1 for the aluminium bridge gates have been calculated from equation 2.21 and compared with the calculated f_1 for the platinum, tantalum and copper bridge gate structures of similar geometries. Aluminium possesses relatively higher ratio of Young's modulus to density and therefore, a stress-free aluminium bridge gate structure will resonate at a higher resonant frequency compared to the ones calculated for the tantalum, platinum or copper bridge gates of the same length and thickness.

Out of these 4 metals, platinum and tantalum are favoured due to their smaller $\frac{E}{\rho}$ ratios and thus, the fabricated platinum and tantalum bridge gates can cover the lower frequency region within the audible range. From the fabrication point of view however, aluminium and tantalum possess the ease of metal deposition and etching techniques compared to copper and platinum. Thus, aluminium and tantalum have been chosen as the materials for the bridge gate structures and the corresponding fabrication processes will be presented in Chapters 3-4.

2.6.2.2 Influence of bridge gate length l_b on resonant frequency f_1

In Figure 2.12, the aluminium and tantalum bridge gate structures of length $l_b = 1.62\ mm - 0.57\ mm$ have been designed to cover the frequency range of $1\ kHz - 8\ kHz$ and $660\ Hz - 5\ kHz$, respectively. The bridge gates have been labelled as $B1 - B10$ according to their length [Table 2.1]. It is necessary to fabricate longer bridge gate structures in order to cover resonant frequencies less than $660\ Hz$. Thus, another ten bridge gate structures have been considered and labelled as $C1 - C10$ with length ranging from $l_b = 5.8\ mm$ to $l_b = 1.8\ mm$. $C1 - C10$ have been designed to cover the frequency range $78\ Hz - 807\ Hz$ for aluminium and $51\ Hz - 530\ Hz$ for tantalum.

The layout design for two arrays of RGTs which employ the bridge gates $B1 - B10$ on a single chip of size $1\ cm \times 1\ cm$ is shown in Figure 2.13. The channel region and source/drain have been assigned for each bridge gate structure. The channels

have been positioned to be at the expected antinode location of the bridge gate. In order to obtain individual control of the RGT devices, the drive and sense circuitry have been designed to connect each bridge gate, source and drain to the bond pads. For bridge gates $C1 - C10$, only one array of RGTs can fit into the chip due to the longer bridge gate structures.

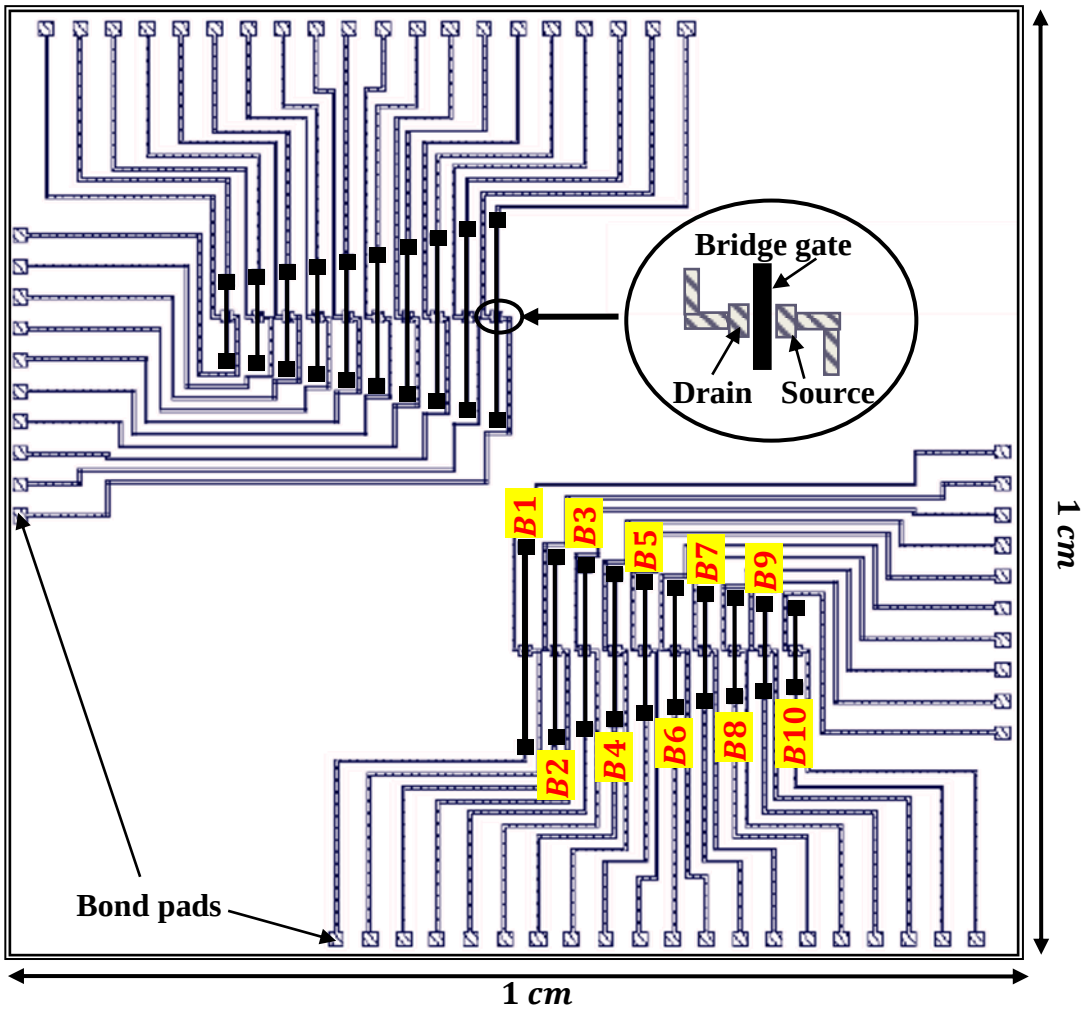


Figure 2.13 *The layout design (top view) for two arrays of RGTs on* $1\ cm \times 1\ cm$ *of chip size, including the drive and sense circuitry that connect each bridge gate, source and drain to the bond pads. Bridge gates* $B1 - B10$ *of length* $l_b = 1.62\ mm - 0.57\ mm$ *are employed for the RGT devices.*

2.6.3 Medium and geometry design for quality factor Q_{10}

The third factor that has been considered for the bridge gate design is the medium that surrounds the structures. Air can be used to dampen the oscillation of the

vibrating bridge gates and the mechanism is known as the squeeze-film damping or air damping [16]. The quality factor of each bridge gate is controlled by the damping of the structure through the pressure and viscosity of air which exists 1) between the bridge gates and 2) between the bridge gate and substrate [16]. The squeeze film damping between the bridge gates has not been studied here as isolated bridge gate analysis has been assumed. Thus, only the squeeze film damping between the bridge gate and substrate is considered in the design.

Batch	$l_b\ (mm)$	f_1	$w_b\ (\mu m)$	$d_i\ (\mu m)$	Q_3
Aluminium					
$B1-B10$	$1.62-0.57$	$1\ kHz-8\ kHz$	5	4	$0.7-6$
$C1-C10$	$5.8-1.8$	$78\ Hz-807\ Hz$	5	4	$0.06-0.6$
Tantalum					
$B1-B10$	$1.62-0.57$	$660\ Hz-5\ kHz$	5	4	$2-24$
$C1-C10$	$5.8-1.8$	$51\ Hz-530\ Hz$	5	4	$0.2-2.4$

Table 2.2 *The design of f_1 and Q_3 with respect to the geometrical dimensions (w_b, d_i and l_b) of the aluminium and tantalum bridge gates.*

The material properties (E and ρ), length and thickness of the bridge gate have been fixed for the design of resonant frequency f_1. Table 2.2 shows the designed values of f_1 with respect to l_b and the metal type. From equation 2.7, the remaining parameters that can be manipulated to design the quality factor Q_3 are the bridge gate width w_b, the distance between the bridge gate and substrate d_i and the viscosity of air ψ. In Table 2.2, assuming $d_i = 4\ \mu m$ which is practical in fabrication, $\psi = 1.845\ e^{-5}\ kg/ms$ [24] and $w_b = 5\ \mu m$, the quality factors of $Q_3 \sim 0.06-6$ for aluminium and $Q_3 \sim 0.2-24$ for tantalum have been estimated with respect to $l_b = 5.8\ mm - 0.57\ mm$.

The lumped element models for aluminium bridge gates $B1-B10$ have been created and the corresponding mechanical frequency responses have been calculated

in order to estimate the quality factor Q_{10}. The frequency responses of aluminium bridge gates $B1 - B10$ with a constant bridge gate width $w_b = 5\ \mu m$ are shown in Figure 2.14. As the bridge gate length decreases from $B1$ ($l_b = 1.62\ mm$) to $B10$ ($l_b = 0.57\ mm$), the quality factor has been estimated to increase from Q_{10}~0.4 to Q_{10}~2.

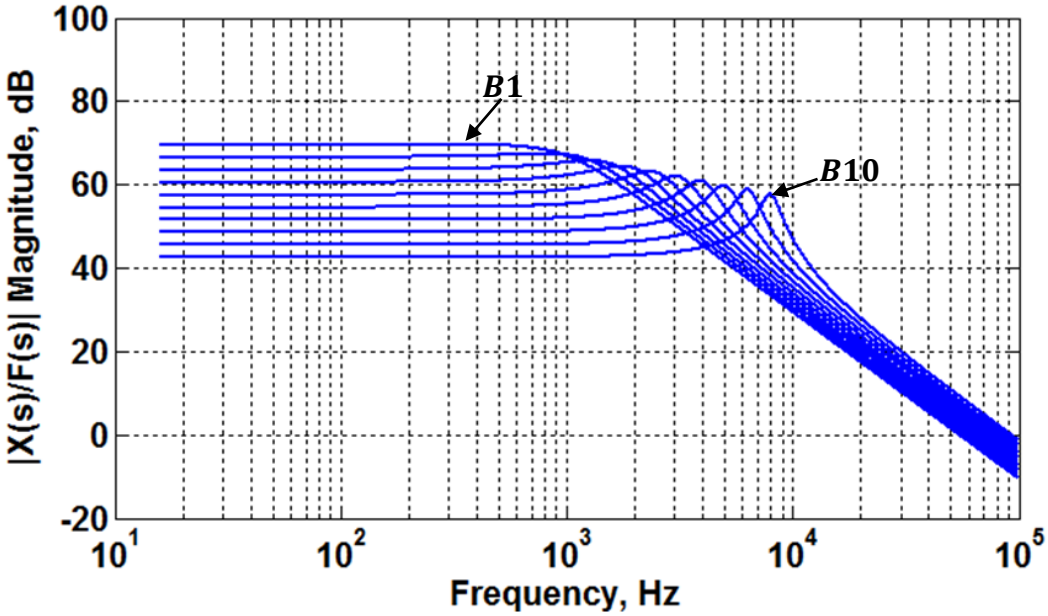


Figure 2.14 *The mechanical frequency responses for aluminium bridge gates at a constant bridge gate width of $w_b = 5\ \mu m$. The quality factor has been estimated to increase from Q_{10}~0.4 to 2 with respect to the decrease in bridge gate length from $l_b = 1.62\ mm$ ($B1$) to 0.57 mm ($B10$).*

2.6.3.1 Influence of bridge gate width w_b on quality factor Q_{10}

From the measured frequency response of cochlea, the quality factor is 1) approximately fixed at each resonant frequency point f_1 and 2) within Q_{10}~$0.6 - 10$. The designed quality factor for the bridge gates can be optimised to follow the frequency response of cochlea. The quality factor range can be reduced by decreasing the distance of the bridge gate to the substrate or employing a more viscous medium, but these actions will affect all bridge gates in the array.

In order to have individual control of the damping for each bridge gate, different width w_b can be assigned for each bridge gate length. High(low) quality factor can

be reduced(increased) by fabricating wider(narrower) bridge gates and thus, bigger(smaller) air squeeze film damping effect could be attained [16]. A constant quality factor of Q_{10}~2 for each aluminium bridge gate can be achieved by varying the bridge gate width from $w_b = 2\,\mu m$ for $B1$ ($l_b = 1.62\,mm$) to $w_b = 5\,\mu m$ for $B10$ ($l_b = 0.57\,mm$) [Figure 2.15]. For tantalum, the bridge gate width is varied from $w_b = 4\,\mu m$ for $B1$ to $w_b = 11\,\mu m$ for $B10$ in order to achieve the constant quality factor of Q_{10}~2.

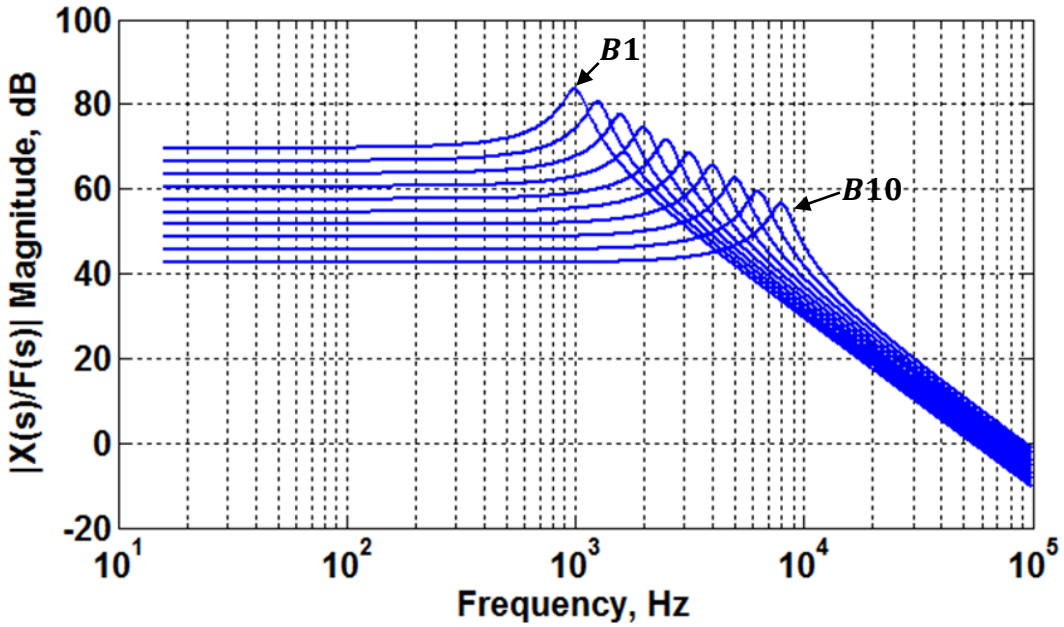


Figure 2.15 *The mechanical frequency responses for aluminium bridge gates with the increase of width from $w_b = 2\,\mu m$ to $w_b = 5\,\mu m$ with respect to the decrease in length from $l_b = 1.62\,mm$ ($B1$) to $0.57\,mm$ ($B10$). The quality factor has been estimated to be constant at Q_{10}~2.*

The number of bridge gates can be increased to cover more frequency points as have been reported by White *et al* in which nearly 3000 suspended beams have been fabricated in order to deliver 3000 channels of frequency information [10].

2.6.4 Channel width W_c design for pull-in voltage V_{pi}

The geometrical dimensions of bridge gate (w_b, t_b, d_i and l_b) have been designed to copy the mechanical response of cochlea (f_1 and Q_{10}). The design for channel

region of RGT is limited as the channel length L_c is set by the bridge gate width w_b and the distance from the channel to bridge gate is given by d_i. Channel width W_c is the only parameter left that can be manipulated to design the 1) pull-in voltage and 2) transconductance of RGT. The equation for pull-in voltage V_{pi} is simplified from equation 2.11 into equation 2.22. The calculated pull-in voltages for aluminium and tantalum bridge gates of length $l_b = 5.8\,mm - 0.57\,mm$ ($B1 - B10$ and $C1 - C10$) with $W_c = 5\,\mu m - 60\,\mu m$ are plotted in Figure 2.16 and the values are tabulated in Table 2.3.

$$V_{pi} = \sqrt{\frac{4.74 E {t_b}^3 {d_i}^3}{\varepsilon_0 W_c {l_b}^3}} \tag{2.22}$$

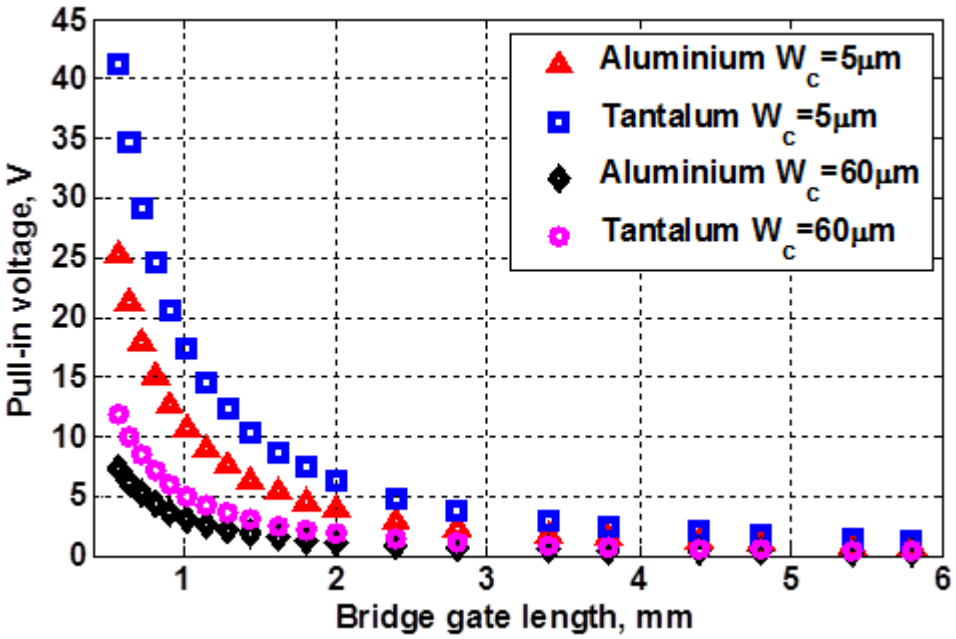


Figure 2.16 *The calculated V_{pi} for aluminium and tantalum bridge gates with respect to the bridge gate length $l_b = 5.8\,mm - 0.57\,mm$ and channel width $W_c = 5\,\mu m - 60\,\mu m$.*

The pull-in voltage range of $V_{pi} = 0.2\,V - 25\,V$ and $V_{pi} = 0.4\,V - 41\,V$ have been calculated respectively for aluminium and tantalum bridge gates, assuming $t_b = 0.5\,\mu m$ and $d_i = 4\,\mu m$ [Table 2.3]. In Figure 2.16, the increase of W_c from 5 μm to

60 μm has been observed to reduce the pull-in voltage. In addition, the pull-in voltage has been observed to decrease with respect to the increase of bridge gate length l_b. Thus, different bridge gate length requires different regime of operation for V_{gs} which has been defined previously as $V_{th} < V_{gs} < V_{pi}$.

Batch	l_b (mm)	f_1	W_c (μm)	V_{pi} (V)
Aluminium				
$B1 - B10$	$1.6 - 0.57$	$1\ kHz - 8\ kHz$	$5 - 60$	$1.5 - 25$
$C1 - C10$	$5.8 - 1.8$	$78\ Hz - 807\ Hz$	$5 - 60$	$0.2 - 4.5$
Tantalum				
$B1 - B10$	$1.6 - 0.57$	$660\ Hz - 5\ kHz$	$5 - 60$	$2.5 - 41$
$C1 - C10$	$5.8 - 1.8$	$51\ Hz - 530\ Hz$	$5 - 60$	$0.4 - 7$

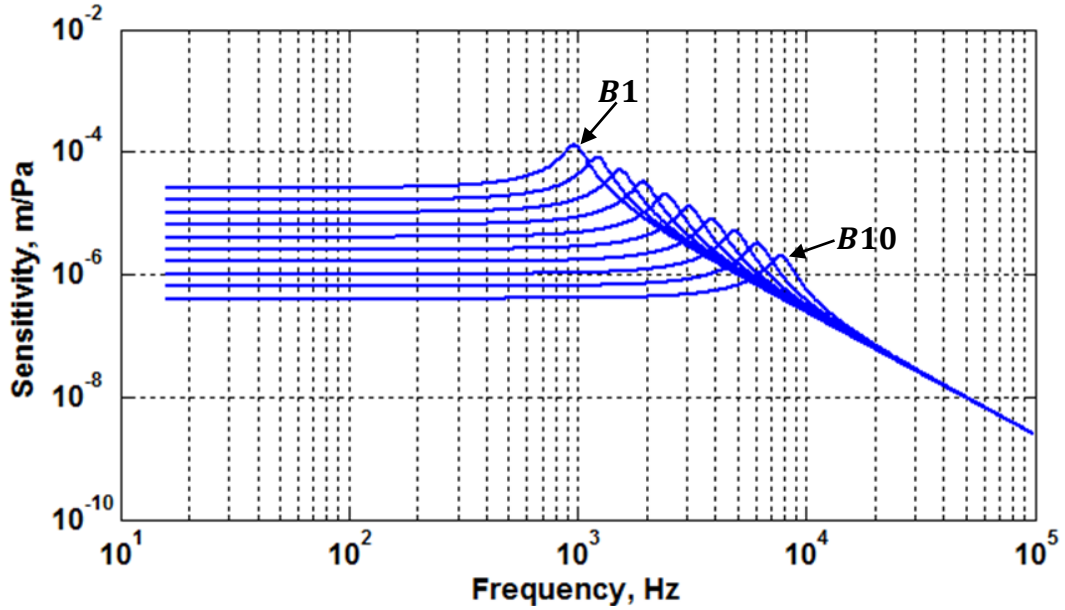
Table 2.3 *The design of pull-in voltage with respect to the geometrical dimensions (W_c and l_b) of the aluminium and tantalum bridge gates, assuming $t_b = 0.5\ \mu m$ and $d_i = 4\ \mu m$.*

It is clear that longer bridge gate with smaller V_{pi} needs to operate at smaller regime of operation for V_{gs} in order to avoid the pull-in condition. Problem arises if the pull-in voltage V_{pi} is smaller than the threshold voltage V_{th}. The decrease in size of W_c will help to increase the pull-in voltage for the bridge gate but at the same time will also reduce the transconductance g_m of RGT [equation 2.20]. Thus, the optimisation of W_c needs to compromise between the values of V_{pi} and g_m. A depletion mode channel instead of enhancement can be employed to solve this problem as the channel is always 'on' and thus satisfies the required $V_{th} < V_{gs} < V_{pi}$ regime of operation [21].

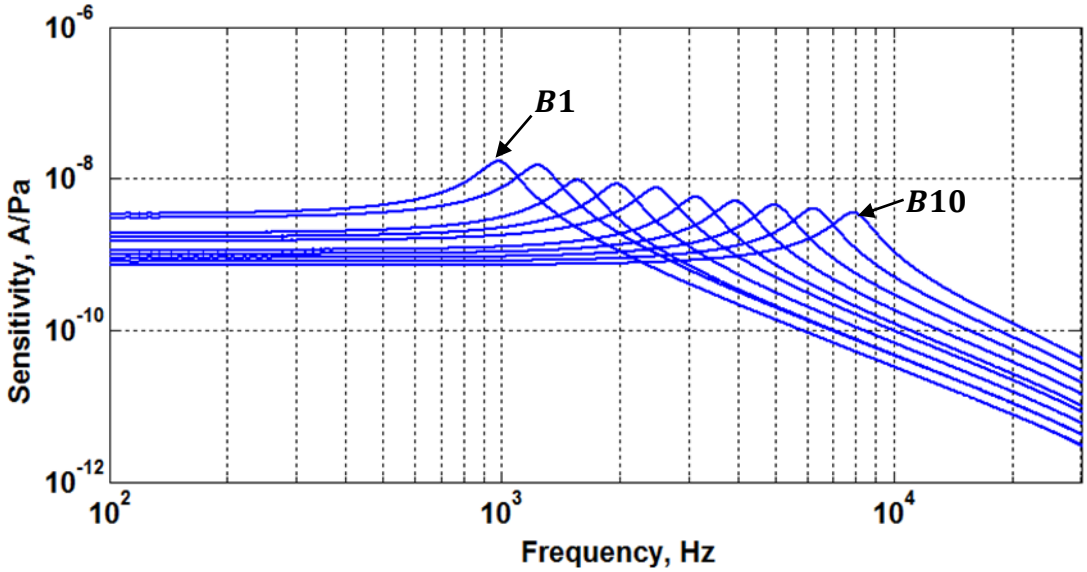
2.6.5 Mechanical and electrical sensitivities of RGT

Finally, the mechanical and electrical sensitivities of RGTs have been estimated using the optimised geometrical dimensions for the aluminium bridge gates $B1 - B10$ [from Figure 2.15(b)] and assuming $W_c = 5\ \mu m$ and $V_{th} = \frac{V_{pi}}{10}$ for the channels.

At $V_{gs} = \frac{V_{pi}}{5}$, the sensitivities have been estimated from the RGTs and plotted in Figure 2.17.



(a) Mechanical sensitivities



(b) Electrical sensitivities

Figure 2.17 *The calculated sensitivities for RGTs with aluminium bridge gates* $B1 - B10$. *(a) The mechanical sensitivities of* $\sim 100\ \mu m/Pa - 2\ \mu m/Pa$ *and (b) the electrical sensitivities of* $\sim 17\ nA/Pa - 4\ nA/Pa$ *have been estimated with respect to the decrease in bridge gate length from* $l_b = 1.62\ mm$ $(B1)$ *to* $0.57\ mm$ $(B10)$.

The mechanical sensitivity has decreased from $\sim 100\ \mu m/Pa$ to $\sim 2\ \mu m/Pa$ with respect to the decrease in bridge gate length from $l_b = 1.62\ mm(B1)$ to $0.57\ mm(B10)$ [Figure 2.17(a)] while for the electrical sensitivity, the value has decreased from $\sim 17\ nA/Pa$ to $\sim 4\ nA/Pa$ [Figure 2.17(b)]. Taking into account the distance of $d_i = 4\ \mu m$ from the bridge gate to substrate, the sound input signal of smaller than $1\ Pa$ should be applied in order to obtain nanometer range of vibration displacements from the bridge gates. The geometrical design for the mechanical bridge gate structure and channel region from Table 2.2 and Table 2.3 will be used to fabricate the RGT devices on $1\ cm \times 1\ cm$ chips. A variation of bridge gate width from $w_b = 2\ \mu m$ up to $w_b = 30\ \mu m$ will be considered and assessed to whether the widths are feasible for the fabrication of the bridge gate structures. Enhancement and depletion mode types of channel will be considered and fabricated in Chapters 5-7.

2.7 Conclusion

The mathematical model for RGT has been developed in order to mimic the mechanical and electrical frequency responses of the cochlea. An array of metal bridge gate structures transduces the sound input signals into mechanical vibrations whilst the channels underneath the bridge gates transduce the mechanical vibrations into small signal drain currents. Lumped element model has been constructed in order to estimate the frequency, quality factor and mechanical sensitivity of the bridge gates operating in air. Then, the lumped element model of the bridge gate has been introduced into the modified drain current model of the MOSFET in order to create the mathematical model for RGT. The estimated electrical current response from RGT has been found to be suitable for neural spike coding and the generated spike signals in spike time domain have been measured to give an adequate representation of the electrical current. The adaptive ability of RGT has been demonstrated by the self-tuning of sensitivity and selectivity with respect to the voltage applied onto the bridge gate V_{gs}. The increase of V_{gs} has amplified the gain of RGT to almost 8.5 times bigger than its initial state and the resonant frequency

has decreased to $\sim 25\,\%$. For safe working operation of RGT, the regime of operation for V_{gs} has been deduced to be smaller than the pull-in voltage and bigger than the threshold voltage.

The material and geometry designs for RGT have been optimised 1) to mimic the mechanical and electrical response of cochlea and 2) to satisfy the limits in the fabrication of RGTs on $1\ cm \times 1\ cm$ chips. For the fabrication of bridge gates, aluminium and tantalum have been chosen due to 1) small $\frac{E}{\rho}$ ratio and 2) straightforward metal deposition and etching techniques. An array of bridge gates with length $l_b = 5.8\ mm - 0.57\ mm$ has been considered for the devices to work within the audible frequency range and the corresponding pull-in voltages V_{pi} have been estimated with respect to the bridge gate length l_b. For aluminium bridge gates, the expected bandwidth of operation is $78\ Hz - 8\ kHz$ with the range of pull-in voltage of $V_{pi} = 0.2 - 25\ V$. Assuming the voltage applied onto the aluminium bridge gates of length $l_b = 1.62\ mm - 0.57\ mm$ to be $V_{gs} = \frac{V_{pi}}{5}$, reasonable mechanical and electrical sensitivities for the RGTs have been estimated to be $\sim 100\ \mu m/Pa\ - 2\ \mu m/Pa$ and $\sim 17\ nA/Pa - 4\ nA/Pa$, respectively with respect to the decrease in l_b.

In Chapters 3-4, investigations will be carried out in order to affirm the feasibility of fabricating the bridge gate structures according to the designed geometries. A reliable fabrication technique for the bridge gate will be introduced. The physical dimensions that can be practically used to construct the bridge gate structure using the proposed fabrication technique will be verified.

Chapter 3: Fabrication process and mechanical characterisation of aluminium bridges

3.1 Introduction

In the fabrication of the resonant gate transistor (RGT), the channel region has to be developed before creating the bridge gate structure. Detailed discussions on the design and characterisation of the *n*-type and *p*-type channel regions will be presented in Chapters 5-7 where the channels have been fabricated, measured and finally integrated with the bridge gates to create RGTs.

In Chapters 3-4, the study will focus on the mechanical part of resonant gate transistor. The fabrication process for the bridge gate structures will be developed in this chapter. The fabricated bridge gate structures without channel underneath will be referred to as bridges. The construction of bridge structure for the RGT requires a sacrificial layer of certain thickness that defines the distance of the bridge from substrate. Anchors are also needed for the bridge to stand on the substrate. Thus, the initial steps of the fabrication process involve the deposition and patterning of the sacrificial layer in order to create the regions to place the bridge anchors. A metal layer is then sputter-deposited on top of the sacrificial layer and patterned into a bridge structure. After patterning the metal bridge, the sacrificial layer is etched away leaving only the overlying structural bridge layer. The employed selective sacrificial layer etch release scheme will etch the underlying sacrificial layer selectively and will neither etch the overlying metal bridge layer nor the drive/sense

metal circuitry layer that runs on the substrate. In the first iteration, photoresist has been selected as the sacrificial layer and aluminium has been used as the metal bridge layer. For the second iteration in Chapter 4, the aluminium will be replaced with tantalum.

The critical point in the fabrication stage of the bridge is the release of the relatively long bridge structure. As has been pointed out in section 2.6.2, the design of MEMS bridges working in audible frequency range ($20\,Hz - 20\,kHz$) requires the structures to be in $0.57\,mm - 5.8\,mm$ range of length. In general, a clean, reliable and damage-free etch release process is desired to ensure that 1) there is no residual of the sacrificial layer left on the channel region and source/drain 2) a gentle process that would not deform the long bridges mechanically and 3) a low temperature process that would avoid thermal damage of the metal bridge, channel region and the source/drain regions. The downstream oxygen/nitrogen plasma etch release technique has been found to be able to offer a clean, reliable and damage-free etch release process. Thus, the downstream oxygen/nitrogen plasma tool will be introduced and compared with other conventional etch release tools/techniques. The study continues with the characterisation of the downstream etch release process. The effects of substrate temperature and flow rates of oxygen and nitrogen gases on the etch rate of photoresist and polyimide sacrificial layer will be investigated in section 3.5.1 and 3.5.2.

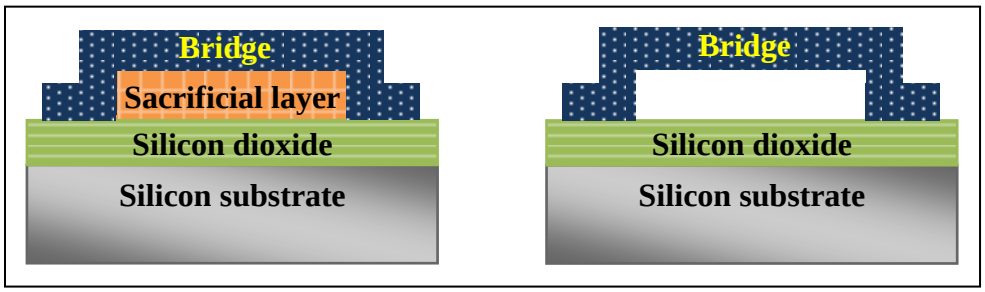
Finally, the mechanical characterisation of the released aluminium bridge structure from the photoresist sacrificial layer will be presented in section 3.6. The frequency responses of the aluminium bridges have been measured and the stress within the aluminium layer has been estimated.

3.2 Selective etch release scheme

Selective wet or dry-etch release scheme is a popular micromachining technique for releasing a mechanical structure [31][34][43][44]. It is a common post-processing

procedure which is used to add a MEMS structure on top of the pre-fabricated CMOS (complimentary metal-oxide-semiconductor) circuitry wafers [31].

In order to create a free-standing bridge structure which is supported by two anchors, a sacrificial layer is used to suspend the bridge above the substrate [Figure 3.1(a)]. The silicon substrate can be insulated from the overlying metal bridge structure by a silicon dioxide layer. Square cavities within the sacrificial layer are defined to accommodate the areas where the bridge will be anchored to the silicon dioxide layer. The overlying structural bridge layer that conforms onto the sacrificial layer has equal thickness on top and on the sidewall of the sacrificial layer. A wet or dry-etch process can be used to selectively remove the sacrificial layer, resulting in a free-standing bridge structure which is cleaved onto the silicon dioxide by its two conformal anchor supports [Figure 3.1(b)]. Using this scheme, there is a freedom of designing the gap size between the bridge and substrate. In Chapter 6, the sacrificial layer will also serve as a masking layer that protects the electrical part of the RGT during the process of constructing the mechanical bridge structure.



(a) Before etch release **(b)** After etch release

Figure 3.1 *Selective etch release process to create a free-standing bridge structure with two conformal anchor supports.*

3.3 Fabrication of aluminium bridges

Ten aluminium bridges of length $l_b = 1.62\,mm - 0.57\,mm$ and labelled as $B1 - B10$ from Table 2.1 with width $w_b = 2\,\mu m - 30\,\mu m$ have been fabricated. The small ratio of Young's modulus to density has made the aluminium metal to be an excellent candidate for the bridges to work within the audible frequency range. Compared to the tantalum metal, aluminium layer can be deposited and patterned

easily. The difficulties with the deposition and patterning of tantalum will be discussed in Chapter 4. Photoresist has been chosen as the sacrificial layer due to the straightforward deposition, patterning and etching techniques of the material.

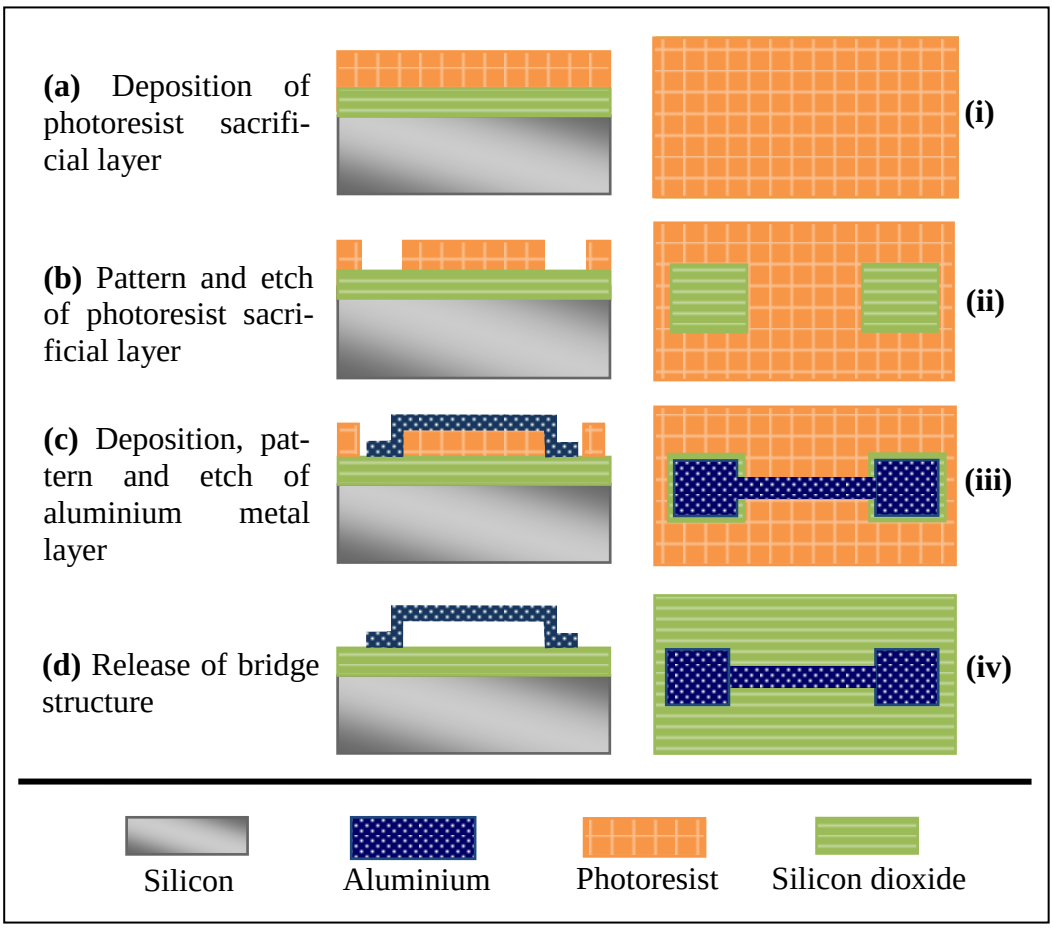


Figure 3.2 *The fabrication process flow for the bridge of RGT.[(a)-(d)] Side view and [(i)-(iv)] top view of the process flow. Aluminium and photoresist have been selected to be the metal bridge and sacrificial layer, respectively.*

3.3.2 Deposition and patterning of sacrificial layer

The process flow for constructing the aluminium bridge structure using photoresist as the sacrificial layer is depicted in Figure 3.2. Starting with the thermally grown silicon dioxide layer (SiO_2) on a 3-inch silicon wafer, the wafer has been heated at 100 ℃ in vacuum oven and applied with the vapour phase of hexamethyldisilazane (HMDS) in order to promote adhesion between the photoresist sacrificial layer onto the SiO_2 surface. In Figure 3.2(a), SPR 220-4.5 photoresist sacrificial layer has been

spun-coated onto the substrate and soft baked at $90\,°C$ and then at $115\,°C$ for $1\,minute$ each. A spin speed of $2500\,rpm$ has been used for the deposition process and the measured thickness of the photoresist sacrificial layer is $\sim 4.4\,\mu m$. The measurement has been performed using Nanospec AFT spectrophotometer. The thickness of the sacrificial layer can be increased to $\sim 6\,\mu m$ or reduced to $\sim 3\,\mu m$ using a spin speed of $1500\,rpm$ and $5000\,rpm$, respectively. The thickness of the sacrificial layer will determine the distance of air gap from the aluminium bridge to the substrate.

Next, the square regions of $120\,\mu m \times 120\,\mu m$ in size have been defined photolithographically using the Karl Suss mask aligner [Figure 3.2(b)]. These patterned areas will accommodate the spaces for the anchors of the bridge. A UV exposure of $35\,s$ is required to pattern the photoresist sacrificial layer of $4.4\,\mu m$ thickness. A proximity contact mode has been used to avoid the stiction between the photoresist sacrificial layer and the 4-inch mask that defines the $120\,\mu m \times 120\,\mu m$ squares. MF26A bath developer has been used to remove the exposed areas and then the wafer has been baked on a hotplate for $15\,minutes$ at $135\,°C$ to drive out any solvent that resides within the sacrificial layer. The temperature has been ramped up from room temperature to $135\,°C$ and after staying at this temperature for $15\,minutes$, the temperature has been ramped down back to the room temperature.

3.3.2.1 Influence of hotplate and oven baking on photoresist sacrificial layer

The advantage of using a hot plate over an oven to vaporise out the solvents from a thick photoresist sacrificial layer is the absence of 'skin effect'. In the oven, the heat is applied onto the outer surface of the photoresist sacrificial layer, forming a seal that can trap the solvent inside the layer. Due to the trapped solvent, any post-processing that involves temperature of $> 100\,°C$ has been observed to cause an adhesion loss of the sacrificial layer from the substrate. In addition, the occurrences of bulk film failures have been observed, in which blisters and bubbles were formed within the photoresist sacrificial layer. The hot plate on the other hand, does not

experience the skin effect problem as the heating process starts from the inside to the outside of the thick photoresist sacrificial layer. It is essential to dry out the photoresist sacrificial layer completely and properly in order to avoid the outgassing of the photoresist that will then distort the structure of the bridge.

3.3.3 Deposition and patterning of aluminium

After baking the photoresist sacrificial layer, the aluminium metal layer of 0.5 μm thickness has been sputter-deposited onto the wafer using the Balzers magnetron sputter system. In the sputter-deposition process, the aluminium target has been bombarded with argon ions to physically break the bonds between the aluminium atoms. These atoms are then deposited onto the wafer and the deposited aluminium has been observed to have good step coverage at 120 $\mu m \times 120$ μm square regions. Afterwards, the aluminium metal layer has been patterned photolithograpically to define the outline of the bridge structures, employing SPR350 Shipley photoresist of 1.6 μm thickness as the mask [Figure 3.3]. Reactive ion etching (RIE) employing $SiCl_4$/Ar plasma in Surface Technology System (STS) metal etcher has been performed on the aluminium metal layer to form the bridge shape [Figure 3.2(c)].

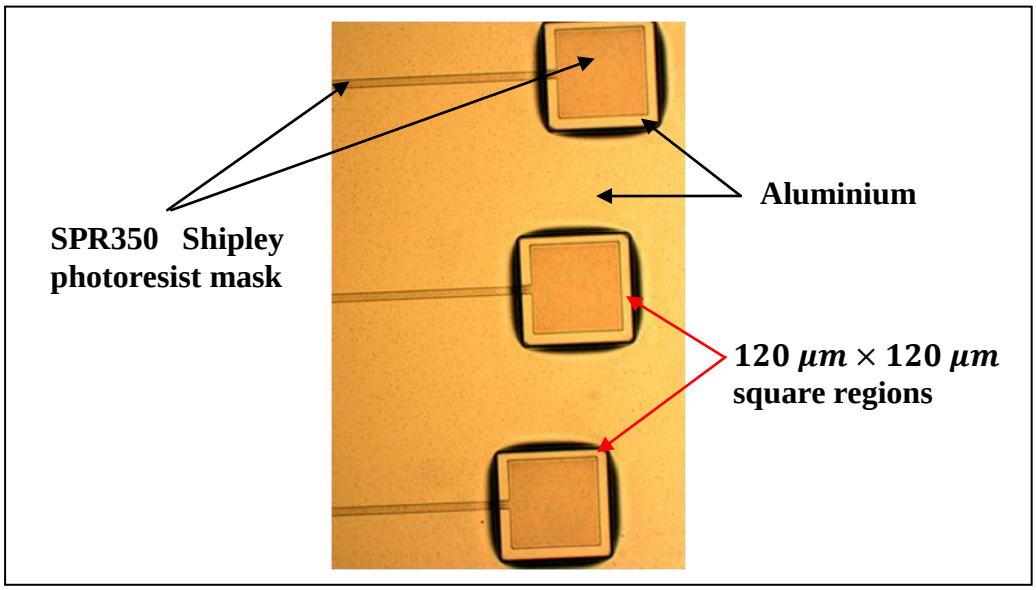


Figure 3.3 *The optical micrograph image of the patterned photoresist mask on the aluminium layer before RIE. The anchors of the bridges are defined within the square regions.*

3.3.4 Etch release of aluminium bridge

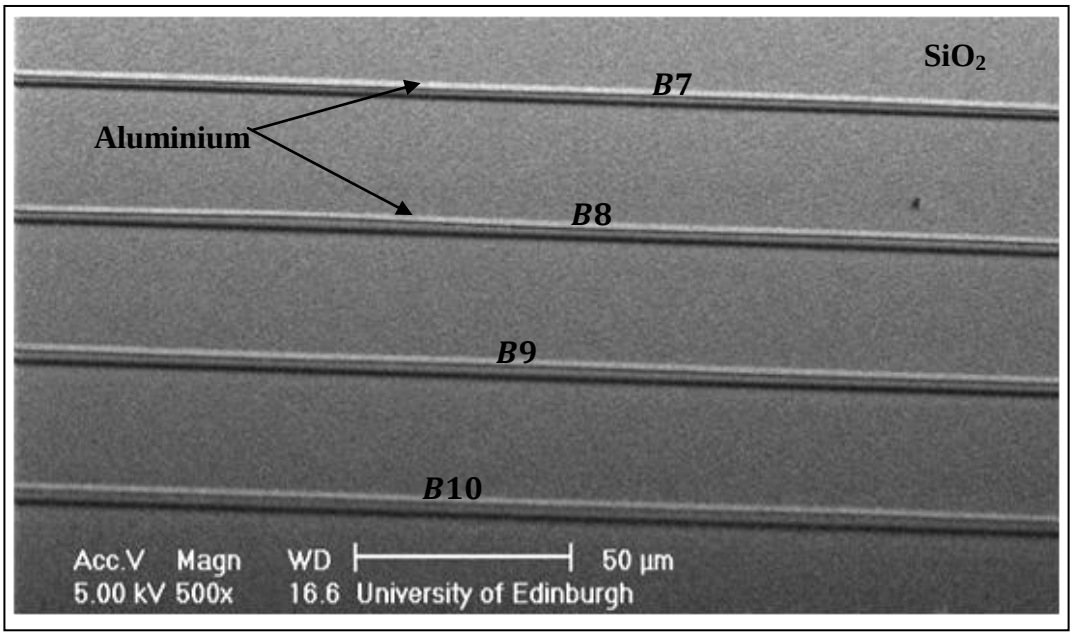
After the aluminium etching step, SPR350 Shipley photoresist mask that defines the bridge structure has been removed using oxygen plasma from the barrel asher. The ashing process has been performed at low temperature for $10\ minutes$. Afterwards, the 3-inch wafer has been cut into $1\ cm \times 1\ cm$ chips using Disco wafer saw. Finally, the aluminium bridges have been released from the photoresist sacrificial layer [Figure 3.2(d)] using the reactive atomic oxygen and nitrogen species in the sacrificial layer etch release tool which employs the downstream plasma configuration. In section 3.5, a detailed investigation on the sacrificial layer etch release tool and the characterisation of the etch release process will be carried out.

The released aluminium bridges have been examined using both optical and scanning electron microscopy (SEM). From the SEM micrograph images, the released aluminium bridges $B7 - B10$ of length $0.91\ mm - 0.57\ mm$ have been observed to be free-standing for width $w_b < 10\ \mu m$ [Figure 3.4(a)-(c)]. The downstream etch release process at $250\ °C$ of substrate temperature, $2000\ sccm$ of oxygen flow rate and $500\ sccm$ of nitrogen flow rate ($sccm$ denotes cubic centimeter per minute at STP) has released the bridges from the photoresist sacrificial layer with an etch rate of $22\ nm/sec$. The etch release process has been considered to be clean and damage-free as there is no photoresist residue on the substrate and the bridge is able to free-stand at the end of the process. The dark lines that appear underneath the bridges have been identified as the bridge shadows.

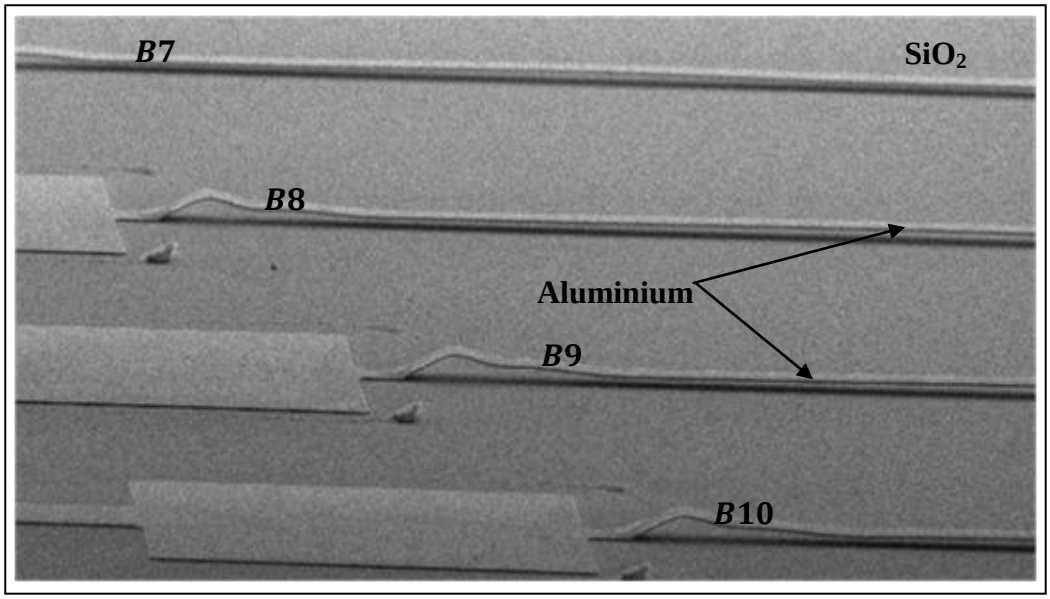
3.3.4.1 Under-exposure of photoresist mask

In Figure 3.4(b) and (c), the residuals that remain at the anchor regions are not the photoresist sacrificial layer but have been identified as aluminium. The reason behind this is the under-exposure of SPR350 Shipley photoresist mask inside the $120\ \mu m \times 120\ \mu m$ squares regions during the photolithography stage. In the beginning, an exposure time of $5\ seconds$ has been used to pattern the SPR350 Shipley photoresist mask of $1.6\ \mu m$ thickness. However, the exposure is not enough to pattern the photoresist mask that resides within the $120\ \mu m \times 120\ \mu m$ square

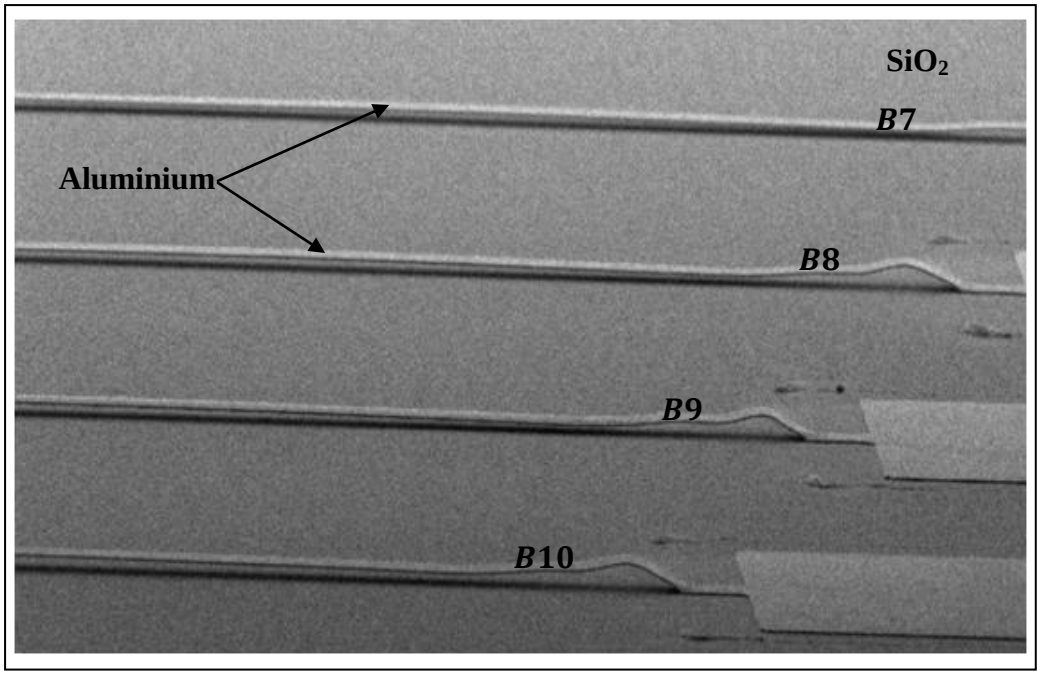
regions of 4.1 μm step down from the surface. This leads to the formation of under-developed photoresist areas which masked away the aluminium from being etched. The unwanted aluminium areas inside the square regions at the bridge anchor could not be completely etched away during the RIE process. This is shown by the optical micrograph image at the anchor region of the released bridge in Figure 3.4(d).



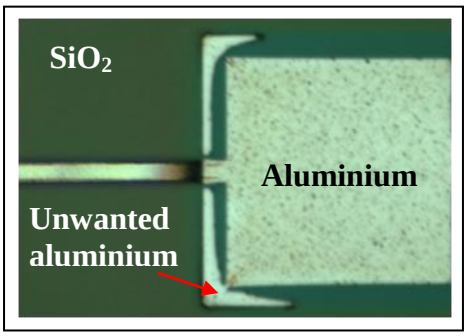
(a) View at the middle region of the bridges



(b) View at the anchor region of the bridges



(c) View at the anchor region of the bridges



(d) View at the anchor region of the bridge

Figure 3.4 *(a)-(c) SEM micrograph images of the released aluminium bridges* $B7 - B10$ *of length* $l_b = 0.91\,mm - 0.57\,mm$. *Bridge width has been measured to be* $w_b \sim 8\,\mu m$, *with thickness of* $t_b \sim 0.5\,\mu m$ *and the distance from bridge to substrate of* $d_i \sim 4.1\,\mu m$. *(d) The optical micrograph showing the top view of the released aluminium bridge with the unwanted aluminium areas at the anchor.*

Thus, the time for the UV exposure of the photoresist mask has been increased in order to remove the unwanted aluminium areas. The optimised time for UV exposure has been found to be $9\,seconds$ and no aluminium residuals around the anchor of the bridge have been seen afterwards.

3.3.4.2 Non-straight/flat aluminium bridges

Figure 3.4(b) and (c) also show that the bridges rise up from their anchors and then come down to settle at a fixed height relative to the substrate. The distance from the bridge to substrate has been measured to be less than the deposited photoresist sacrificial layer thickness of 4.4 μm. Figure 3.5 shows the surface profiles of the patterned photoresist sacrificial layer measured by DEKTAK 8000 surface profilometer at the anchor region before and after the sacrificial layer baking stage. Before baking, the thickness of the sacrificial layer has been measured to be 4.4 μm and the scanned surface profile of the layer is seen to be uniform without waviness. After being baked for 15 $minutes$ at 135 ℃, the thickness of the sacrificial layer has reduced to ~4.1 μm. In addition, bumps have been observed to appear at the edge of the patterned sacrificial layer. Consequently, the constructed bridge on the patterned sacrificial layer after the baking step possesses bumps after the anchors. The thickness, uniformity and surface profile of the patterned photoresist sacrificial layer will determine the features of the constructed bridge.

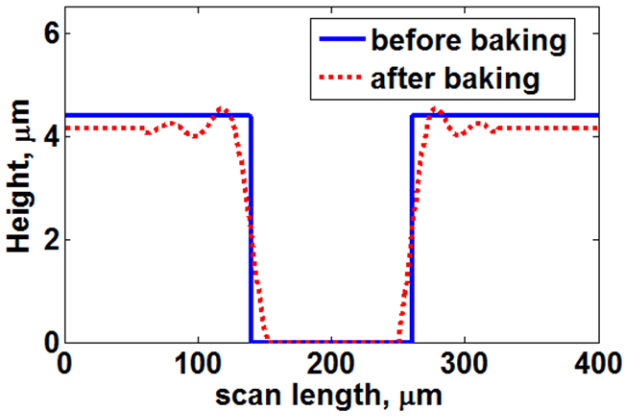


Figure 3.5 *The surface profiles of the deposited and patterned photoresist sacrificial layer at the* 120 $\mu m \times 120$ μm *square regions before and after the baking step.*

3.3.4.3 Non free-standing aluminium bridges

From the fabrication results, the released aluminium bridges with bridge width of $w_b < 10$ μm and length of 1 $mm - 0.57$ mm $(B6 - B10)$ have been observed to be free-standing while the released aluminium bridges of length longer than 1 mm

($B5 - B1$) have been seen to sag down and touch the substrate after the anchors. The same phenomenon has been observed to happen when the aluminium bridges of bridge width $w_b = 10\ \mu m - 30\ \mu m$ and length $1.62\ mm - 0.57\ mm$ ($B1 - B10$) are released, an example is shown by Figure 3.6. Stress-related issue discussed in section 3.6 has been suspected to contribute to the sagging and collapsing of the bridges. Therefore, in order to fabricate a free-standing aluminium bridge structure that has been sputter-deposited from the Balzers, the bridge width should be less than $10\ \mu m$ for the maximum bridge length of $1\ mm$.

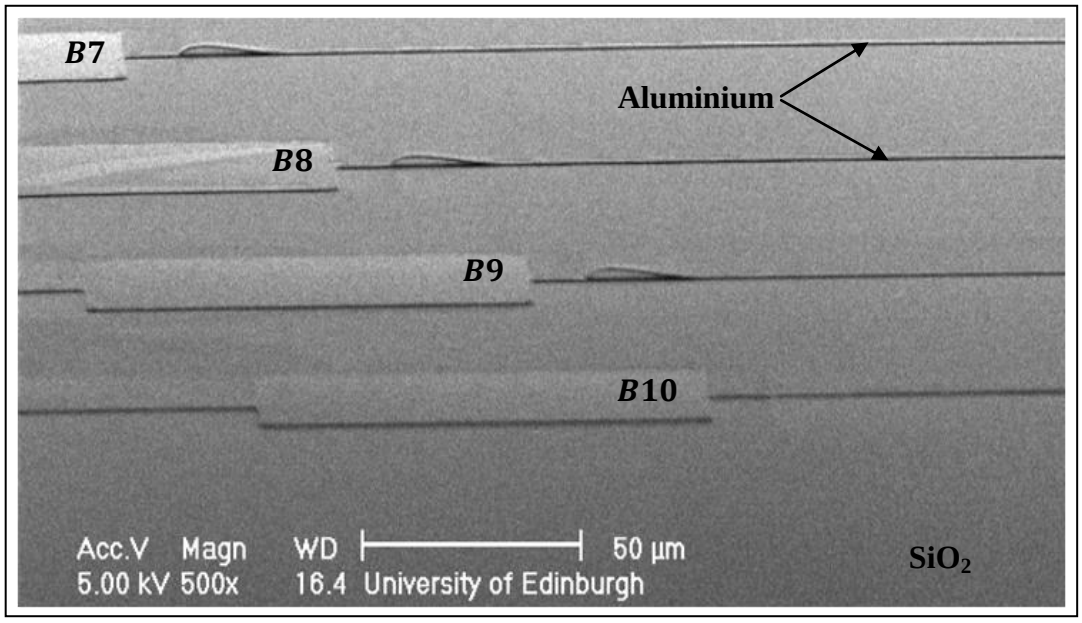


Figure 3.6 *SEM micrograph images of the released aluminium bridges* $B7 - B10$ *of length* $0.91\ mm - 0.57\ mm$. *The bridge width has been measured to be* $\sim 10\ \mu m$ *and the released structures have been observed to sag and touch the substrate.*

The developed sacrificial layer etch release technique using the downstream oxygen/nitrogen plasma tool has been considered to be reliable with the capability of releasing the considerably long bridges (up to $1\ mm$). It is believed that the etch release process does not contribute to the sagging of the bridges, as the limitations from the metal itself i.e. stress has been inferred to cause the sagging of the bridges. The developed technique is introduced and compared with other etch release techniques in the next section.

3.4 Mechanism of etch release

In general, the etching method can be categorised into wet and dry etching techniques [48][49][50]. In wet etching, liquid chemical mixtures are used to react with the material to be etched, producing soluble products that can dissolve away. Alternatively, gas can be used in dry etching where plasma is employed typically. The plasma is a fully or partially ionised gas that is composed of ions, electrons and neutrals as the reactive species for the etching process. There are also several other gas-phase etchants which do not involve plasma for example xenon difluoride gas (XeF_2) and hydrogen fluoride vapour (HF) [50].

There are three types of plasma-assisted etching process. One is 'plasma etching' and refers to a process that depends only on a chemical reaction between the plasma and the material to be etched [48]. On the other hand, a 'reactive ion etching' utilises both the chemical reaction and physical bombardment by the energetic ions from the plasma. Finally, 'sputter etching' is a purely physical ion bombardment etching process [48].

3.4.1 Wet-etch release process

In the beginning, a wet-etch release method has been considered to release the aluminium bridges. 98% fuming nitric acid has been used to etch the photoresist sactificial layer for $10\ minutes$. It is an isotropic etching where the etch rate is equal in all directions [52]. After etching the photoresist sacrificial layer, the released aluminium bridges have to be rinsed with DI water and dried in air. Drying in air has led the liquid surface tension to pull the bridge and cause the stiction of the bridge onto the substrate.

Thus, a critical point drying system is utilised to dry up the bridges. The system uses the physical properties of the liquid carbon dioxide CO_2 with the critical point at $31\ °C$ and $1072\ psi$ to rinse the bridges without causing stiction. The densities of liquid and vapour phase for CO_2 become equal at the supercritical region resulting in zero surface tension. The released and dried aluminium bridges have been observed to be free-standing in clean condition with no photoresist residuals on the substrate.

However, the overall wet-etch release process consumes more time compared to the dry-etch release process due to the drying technique. After rinsing the etch released aluminium bridges with DI water, isopropanol (IPA) is then used to wash away the DI water. As CO_2 is not miscible in DI water, IPA acts as the intermediate medium. In the critical point drying system, IPA will be washed away by the high pressured CO_2 liquid. The temperature for CO_2 is increased in order to transform itself from the liquid state into gas until its pressure reaches the critical point. The pressure is then released gradually by escaping the CO_2 gas, leaving the dried aluminium bridges. The drying process took more than 1 $hour$.

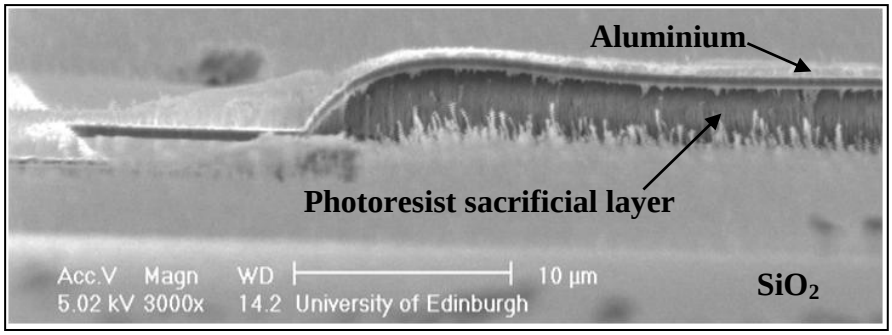
3.4.2 Anisotropic RIE dry-etch release process

In dry-etch release process of the aluminium bridges from the photoresist sacrificial layer, the oxygen plasma can be used as the reactive species. In a common RIE setup, there are two parallel electrodes and the wafer is placed on one of them. An electric field is applied between the two electrodes to create the plasma and to accelerate the ions towards the wafer, creating a vertical etching. The etching of the photoresist sacrificial layer is dominated by the oxygen ion bombardment compared to the chemical reaction from the oxygen radicals [52].

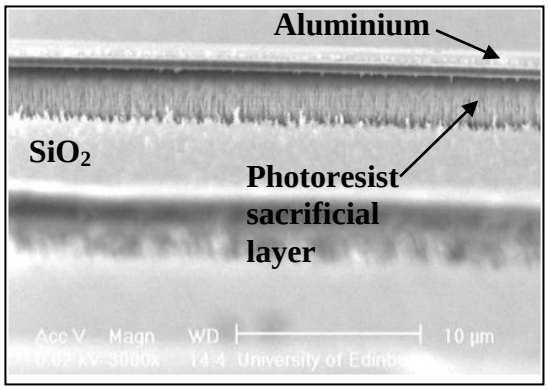
Figure 3.7(a)-(b) show the etched photoresist sacrificial layer from the aluminium bridge structure using RIE technique. The photoresist sacrificial layer which is normal to the direction of ion bombardment has been etched away and the part underneath the bridge has been observed to remain. RIE technique should not be employed to release the aluminium bridges from the photoresist sacrificial layer since it is an anisotropic process in which the etching only occurs in the vertical direction [52].

3.4.3 Isotropic dry-etch release process

A barrel type etcher has been utilised in an attempt to etch release the aluminium bridges using the isotropic dry-etching technique. The oxygen ion bombardment on the photoresist sacrificial layer is small since the wafer is not grounded or biased.



(a) At the anchor region of the bridge



(b) At the middle region of the bridge

Figure 3.7 *(a)-(b) Anisotropic oxygen RIE technique on the photoresist sacrificial layer is unable to release the aluminium bridge.*

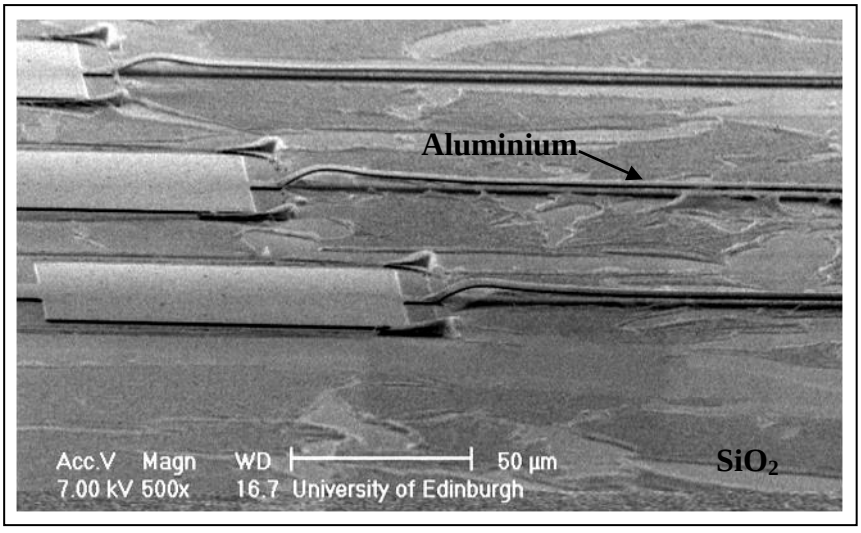


Figure 3.8 *Isotropic oxygen plasma etching of the photoresist sacrificial layer in the barrel asher managed to release the aluminium bridges but the process is not clean.*

Low energy ions are accelerated towards the wafer [52]. Thus, the anisotropic etching process due to oxygen ion bombardment is not significant [52]. Isotropic oxygen 'plasma etching' is more dominant in the barrel type etcher. Figure 3.8 shows the release of the aluminium bridges from the photoresist sacrificial layer using the isotropic oxygen plasma in the barrel asher. The bridges have been observed to be released but the process is slow and not clean as there is still photoresist residual left on the substrate after 1 $hour$ of etch release process.

3.4.4 Downstream isotropic dry-etch release process

The radiation from a plasma has been reported to cause surface damage on the wafer as the wafer is subjected to the energetic ion bombardment [32][36][40][45] [49][51][52]. In addition, the induced current within the wafers due to the charging effect can cause the fabricated electrical components in the wafer especially for the thin gate oxide devices to breakdown [52]. This plasma-induced damage can be eliminated by employing the downstream etch release configuration tool [36]. The plasma is generated at a remote location before being extracted towards the device. Thus, the devices will not be exposed to the ion bombardment and electric field environment that is used to generate the plasma.

3.4.4.1 Downstream oxygen/nitrogen plasma tool

The downstream oxygen/nitrogen plasma tool has been used to dry-etch release the aluminium bridges and the relatively long aluminium structures have been observed to be free-standing in Figure 3.4 in section 3.3.4. This sacrificial layer etch release module is manufactured by MEMSSTAR and can be used generally to etch polymers like photoresist and polyimide [Figure 3.9]. The tool consists of a plasma unit, process monitor, vacuum system, chamber unit and control system [33].

The oxygen and nitrogen gases are fed into the plasma unit where the reactive atomic oxygen and nitrogen species are created. The generated plasma is then extracted downstream from the plasma unit towards the chamber unit where the devices reside. The continuous flow of the reactive species will react with the sacrificial layer and

the volatile products from the reaction are then pumped away from the chamber. The etching will depend mainly on the chemical reaction between the extracted reactive species and the photoresist sacrificial layer, thus creating a 'plasma etching' process.

No oxygen ion bombardments have occurred as the ions recombined before reaching the wafer. At the same time, the reactive atomic oxygen also recombined but a slower rate compared to the ions [35][36]. Thus, nitrogen has been added to avoid this recombination mechanism and simultaneously help to increase the generation of reactive atomic oxygen, leading to higher etching rate [36].

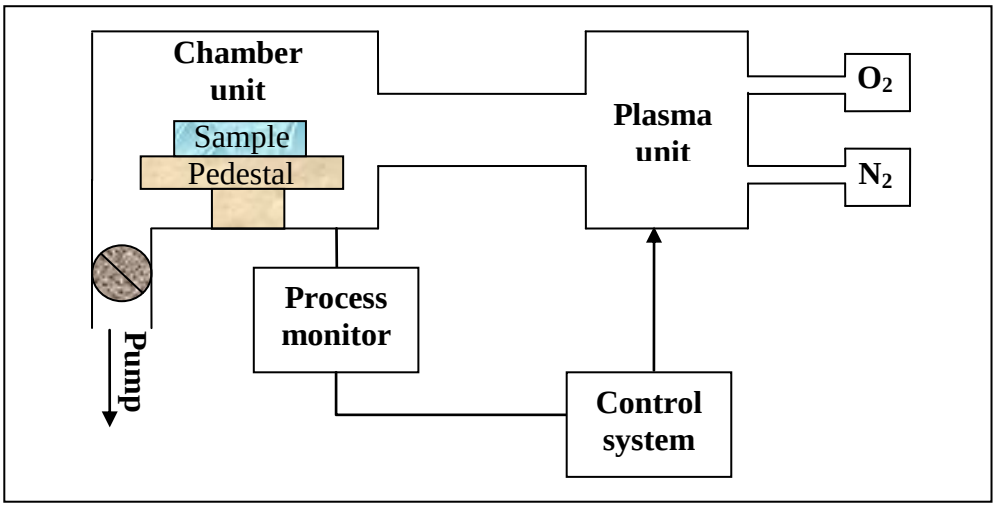


Figure 3.9 *Block diagram of downstream oxygen/nitrogen plasma tool which has been manufactured by MEMSSTAR to etch polymers.*

The temperature of the sample substrate and the pressure within the chamber can be monitored and controlled directly. The temperature is measured using a thermocouple which is attached to the pedestal and located close to the device sample. The temperature of the sample can be optimised by changing the temperature of the pedestal. The chamber is pumped down using a vacuum pump and the pressure inside the chamber is measured using a baratron. The chamber pressure depends on the continuous flow rates of the oxygen/nitrogen gases. The developed technique is able to ensure a fast, clean and damage-free etch release process for the aluminium bridges. The characterisations of such technique on the

photoresist and polyimide sacrificial layers are presented in the next section. The effects of substrate temperature and the flow rates of the reactants have been investigated.

3.5 Sacrificial layer etch release characterisation using downstream oxygen/nitrogen plasma tool

The characterisation for photoresist sacrificial layer etch release process with respect to temperature has been carried out within the range of $105\ °C$ to $175\ °C$, while for polyimide, the etch release process has been studied between $205\ °C$ and $265\ °C$. The influences of temperature and oxygen/nitrogen gas flow rates on the undercut etch rates and the profiles of etch front for photoresist and polyimide test structures have been presented.

3.5.1 Photoresist sacrificial layer etch release

In order to characterise the etch release process of aluminium bridges from the photoresist sacrificial layer, test structures have been fabricated in Figure 3.10. The test structure consists of photoresist etch channels of different width/etch opening size beneath a thin layer of aluminium mask [25][43][44]. The photoresist etch channels with $3\ \mu m - 100\ \mu m$ of etch channel width/etch openings have been fabricated. First, the SPR 660-1.0 photoresist sacrificial layer with $0.8\ \mu m$ of thickness has been spun-coated onto a glass wafer [Figure 3.10(a) and (i)]. Subsequently, the photoresist has been patterned photolithographically into etch channels and baked on a hotplate at $115\ °C$ for $2\ minutes$ [Figure 3.10 (b) and (ii)].

Next, aluminium of $1\ \mu m$ thickness has been sputter-deposited onto the substrate [Figure 3.10(c) and (iii)] and patterned photolithographically to define the etch opening windows. RIE has been performed on the aluminium layer in order to create the etch opening windows [Figure 3.10(d) and (v)]. After the aluminium etching step, the wafer has been diced into $1.0\ cm \times 0.5\ cm$ of sample size. The sample is then placed onto the pedestal inside the chamber unit of the downstream oxygen/nitrogen plasma tool and the incoming reactive atomic oxygen and nitrogen

etched the photoresist sacrificial layer underneath the aluminium mask [Figure 3.10(e) and (vi)].

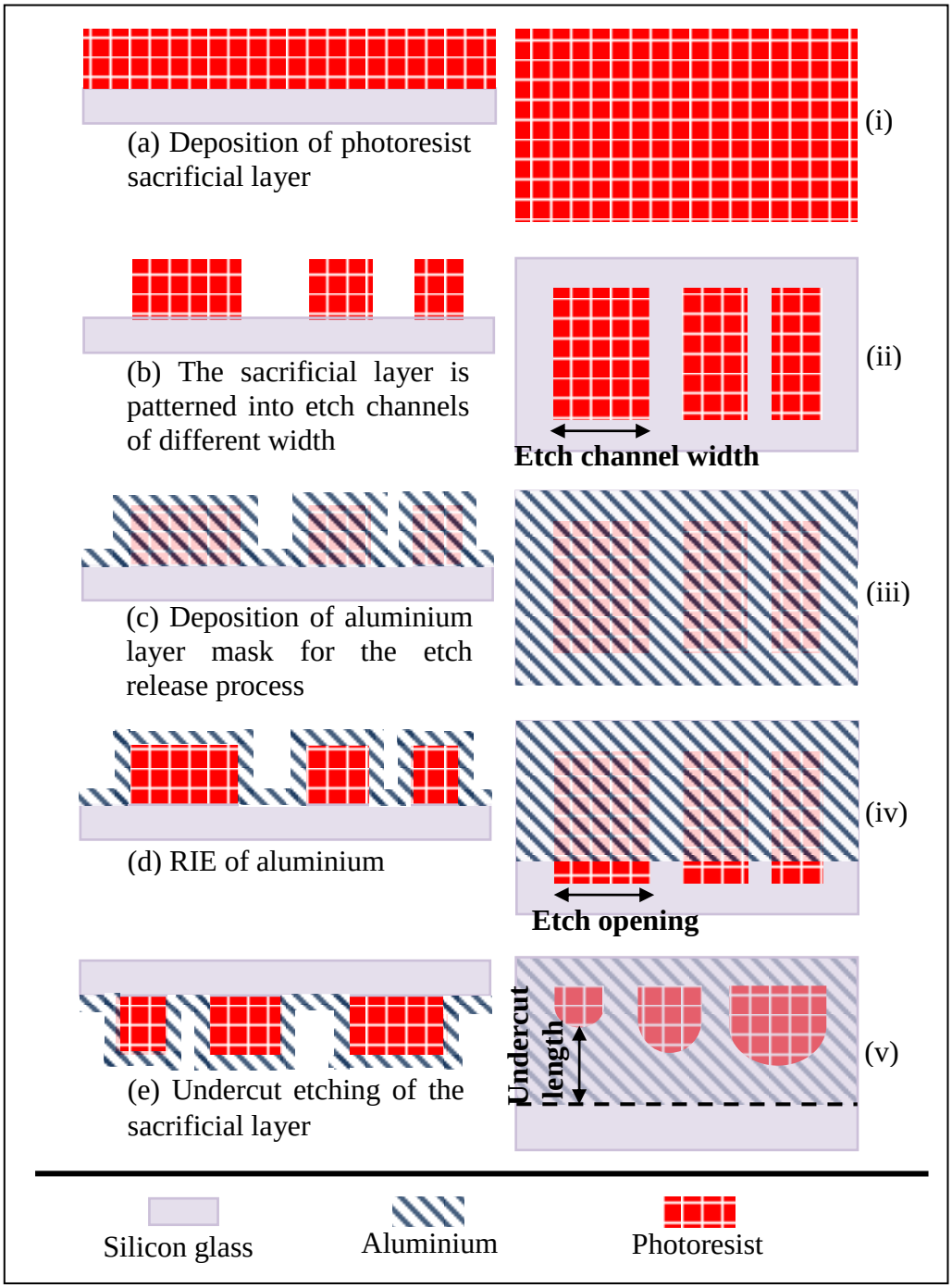
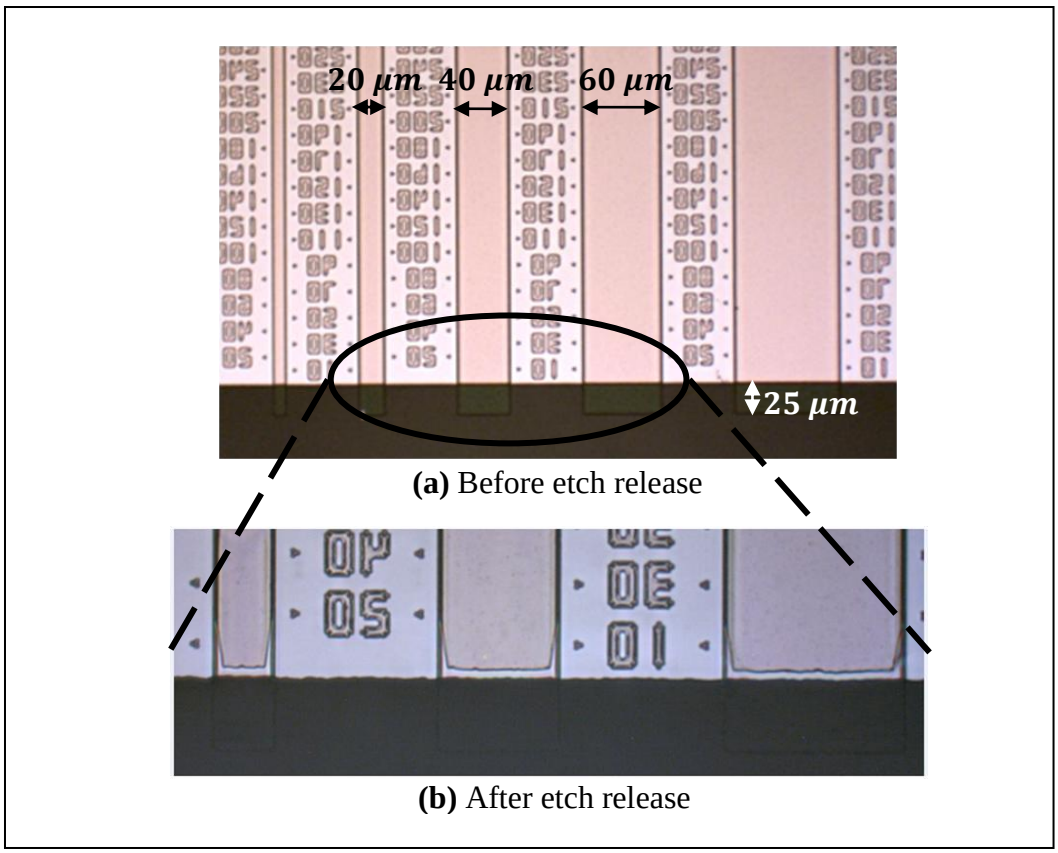


Figure 3.10 *Fabrication and etch release process of the test structure used for the characterisation of photoresist sacrificial layer etch release process. [(a)-(e)] Cross sectional and [(i)-(v)] top view of the fabrication process.*

The undercut lengths have been measured from the back side of the transparent glass wafer using the optical microscope [Figure 3.10(e) and (v)].

3.5.1.1 Photoresist etching reaction

The fabricated photoresist etch channels underneath the aluminium mask layer, before and after being etched in the plasma tool are shown in Figure 3.11. The etching process starts from the exposed 25 μm length of photoresist etch channel and continues towards the etch opening window, etching the photoresist underneath the aluminium mask layer.



(a) Before etch release

(b) After etch release

Figure 3.11 *The photoresist etch channels with different widths (a) before and (b) after the etching process.*

The etching reaction involves 1) the diffusion of reactive species towards the sacrificial layer's surface, 2) the adsorption of reactive species onto the surface, 3) the surface chemical reactions between the reactive species and sacrificial layer,

forming the volatile by-products, 4) desorption of the products from the surface and finally 5) the removal/diffusion of the products away from the surface [34]. The volatile stripping products from the reaction between oxygen plasma and photoresist have been reported to be made up of CH, CO and OH compounds.

The emanated species from oxygen plasma are made up mostly by the atomic oxygen (O), smaller quantities of positive and negative oxygen ions (O_2^+, O^-), molecular oxygen (O_2), excited states of molecular oxygen (O_2^*) and free electrons (e) [41][32]. The generation of reactive atomic oxygen O is due to the dissociation of the excited molecular oxygen O_2^* through the following reaction [32][35];

$$O_2 + e \rightarrow O_2^* \rightarrow 2O + e \tag{3.1}$$

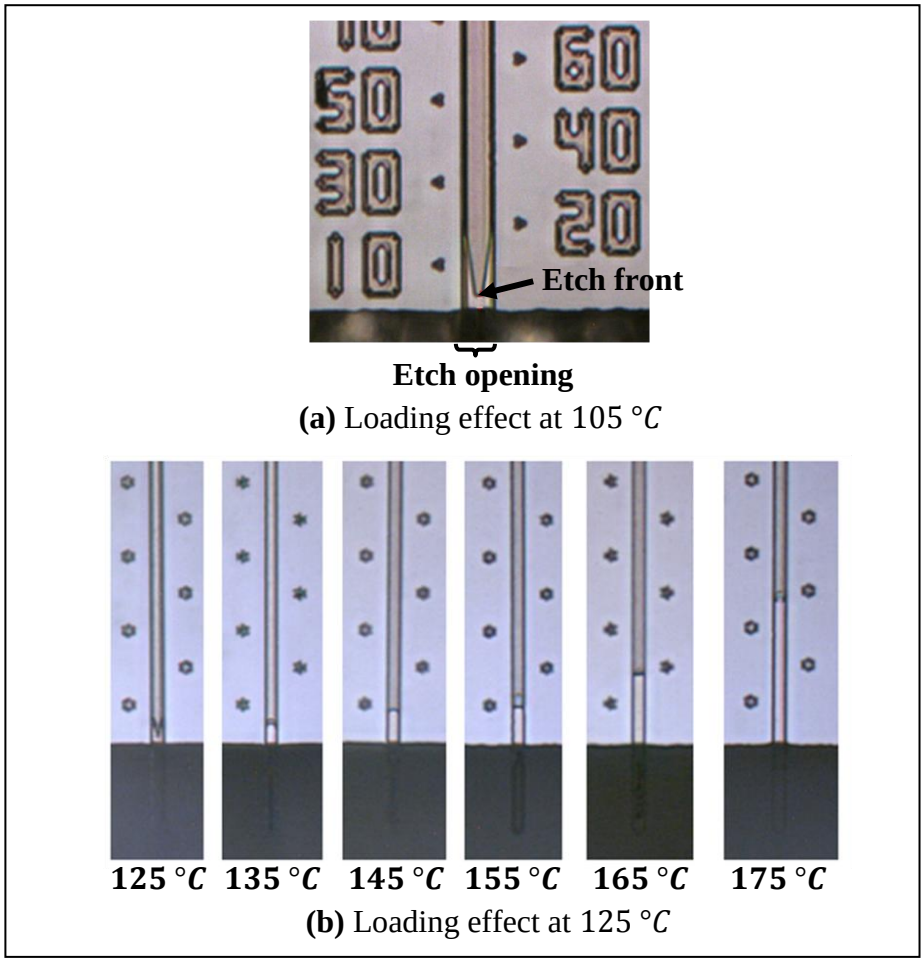
In downstream configuration, the ionic species have been reported to disappear due to the recombination mechanism while being transported to the chamber leaving only the atomic oxygen to react with photoresist [41][36][35]. Since the atomic oxygen also recombines while being transported (but at a slower rate), the nitrogen gas has been added to reduce/stop the recombination mechanism.

3.5.1.2 Influence of substrate temperature on loading effect

The influence of substrate temperature ($105\,°C - 175\,°C$) on the photoresist sacrificial layer etch release process has been measured. After the base pressure in the chamber reaches $0.01\,Torr$, $1000\,sccm$ of oxygen and $100\,sccm$ of nitrogen have been introduced into the plasma unit, with a power fixed at $5\,kWatt$. The pressure in the chamber is fixed at $0.936\,Torr$ which corresponds to the flow rates of oxygen and nitrogen gases. For a fixed pumping speed, the pressure in the chamber can be increased by increasing the flow rates of the gases. At fixed flow rates and pressure, the number of O atoms delivered per unit time is constant [42].

The profiles of the etched photoresist channels at different temperatures are shown in Figure 3.12. In Figure 3.12(a), the etch release process has been performed for $70\,minutes$ on a photoresist etch channel of $5\,\mu m$ width at $105\,°C$. It is observable

that larger etch rate has occurred at the sides of the etch channel, probably due to the presence of loading effect (loss of oxygen atoms) within the etch channel [45][46].



(a) Loading effect at 105 °C

(b) Loading effect at 125 °C

Figure 3.12 *(a) Loading effect within the photoresist etch channel after the etch release process at* 105 °C*. The undercut etch length is measured from the etch opening to etch front location. (b) For* 125 °C − 175 °C *of temperature range, loading effect within etch channel only occurred at* 125 °C.

The loss of oxygen atoms at low substrate temperature might be related to the oxygen atom recombination mechanism reaction [38]. Campbell *et al* have measured the increase of oxygen atom recombination reaction as the temperature decreases [37][38]. In this case, the distance from etch opening to etch front has been taken as the undercut etch length. In Figure 3.12(b), the etch release process has been performed on the photoresist etch channels of 3 μm width at temperatures

of $125\ °C - 175\ °C$ for $70\ minutes$. Loading effect happens at $125\ °C$ of substrate temperature while at $135\ °C - 175\ °C$, the etching is fast and uniform across the etch channel width with no loading effect observed within the etch channel.

3.5.1.3 Influence of substrate temperature on etch rate

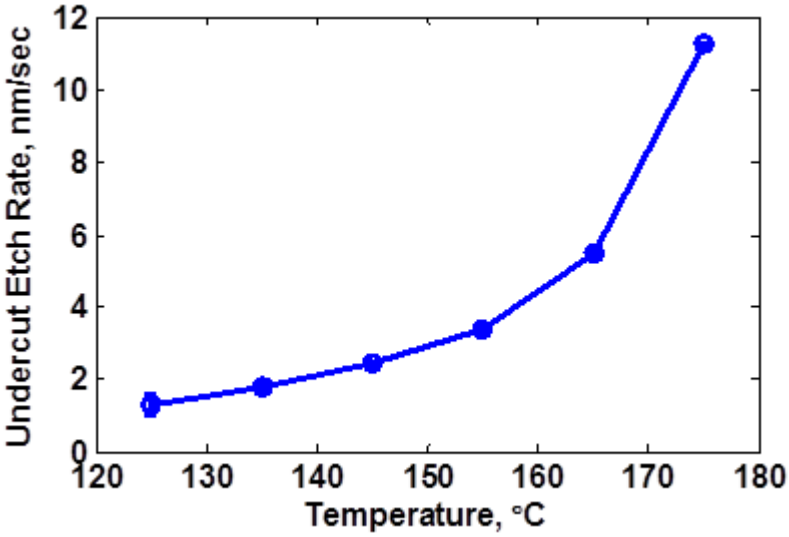
The undercut etch rate k_p has been calculated from the measurement of undercut etch length over the etching duration. Figure 3.13(a) shows the measurement of the undercut etch rate as a function of substrate temperature for etch channel width of $3\ \mu m$ under $1000\ sccm/100\ sccm$ of oxygen/nitrogen flow rates. The undercut etch rate has been observed to increase exponentially as the substrate temperature increases. Assuming linear kinetics of photoresist etching reaction, k_p can be expressed in Arrhenius form [equation 3.2], where E_a is the activation energy of surface reaction, T is the absolute value of substrate temperature, k_{p0} is the pre-exponential factor value and K is the gas constant [35][45].

$$k_p = k_{p0} e^{\frac{-E_a}{KT}} \tag{3.2}$$

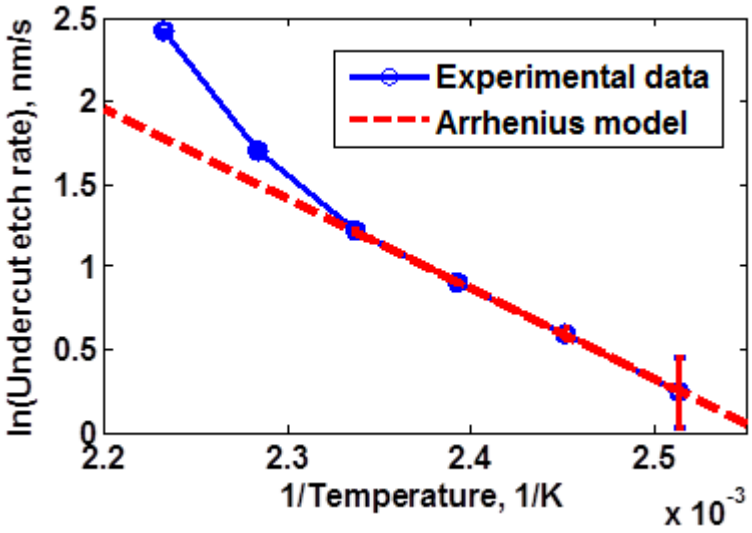
The surface activation energy of the photoresist etch release process E_a has been deduced by fitting the measured undercut etch rate with the linear form of Arrhenius equation [Figure 3.13(b)].

Two data points from the highest substrate temperature have been excluded from the least squares fitted line. The photoresist etch channels, particularly for width $> 40\ \mu m$ have been observed to expand and flow out from the etch openings at temperatures above $160\ °C$. Thus, deviations of the two highest temperature points from the fitted line might suggest some significant property changes of the photoresist which has been baked at a relatively low temperature ($115\ °C$) compared to the substrate temperature during etch release process [35]. In this study, the temperature regime for photoresist etch release has been restricted to $< 180\ °C$. From the gradient of the fitted line in Figure 3.13(b), the activation energy for photoresist is $E_a = 45.32\ kJ/mol$. T. H. Lin *et al* have reported $E_a = 35.98\ kJ/$

mol for photoresist etching under the etch condition of 2000 $sccm$ of oxygen gas flow rate and 5.3 $Torr$ of pressure [40].



(a) Measured undercut etch rate with respect to temperature



(b) Fitting of linear Arrhenius model into measurement data

Figure 3.13 *(a) Measurement of the exponential increase in undercut etch rate for photoresist as a function of temperature with* 3 *μm of etch opening and* 1000 $sccm/100$ *sccm of oxygen/nitrogen. (b) The corresponding Arrhenius plot from the measurement data in (a) is fitted to the linear Arrhenius model.*

Different photoresist deposition processing has been carried out in their work where the photoresist has been deposited on 51 mm diameter of silicon wafers and then

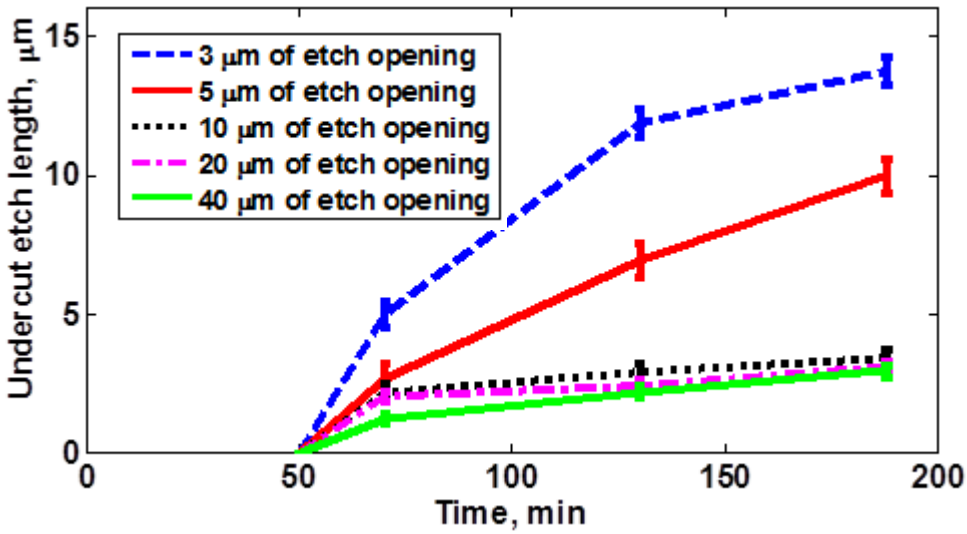
baked at higher temperature (125 ℃) and longer time ($0.5\ hour - 1\ hour$) compared to our fabrication process.

The lower activation energy reported by T. H. Lin might be due the fact that the etch release process has been performed at higher substrate temperature regime (until $230°C$) and higher oxygen gas flow rate. In addition, it might be also due to the bigger size of the tested sample compared to our chip sample, as higher values of E_a have been reported for small test substrates [40]. Cook *et al* have measured an average activation energy of $E_a = 48.50\ kJ/mol$ under $101\ sccm$ of oxygen flow rate for $2\ cm \times 2\ cm$ of photoresist sample which has been baked for $40\ minutes$ at $140\ °C$ [42]. The measured E_a from our work and other researchers could not be compared directly due to the different deposition and etch conditions of the photoresist. Overall, the etching rate for polymers like photoresist and polyimide depends on four factors; 1) the baking/curing time and temperature of the polymers, 2) the concentration of oxygen which is delivered to the polymers' surface, 3) the substrate size and 4) the substrate temperature during the etch release process [40].

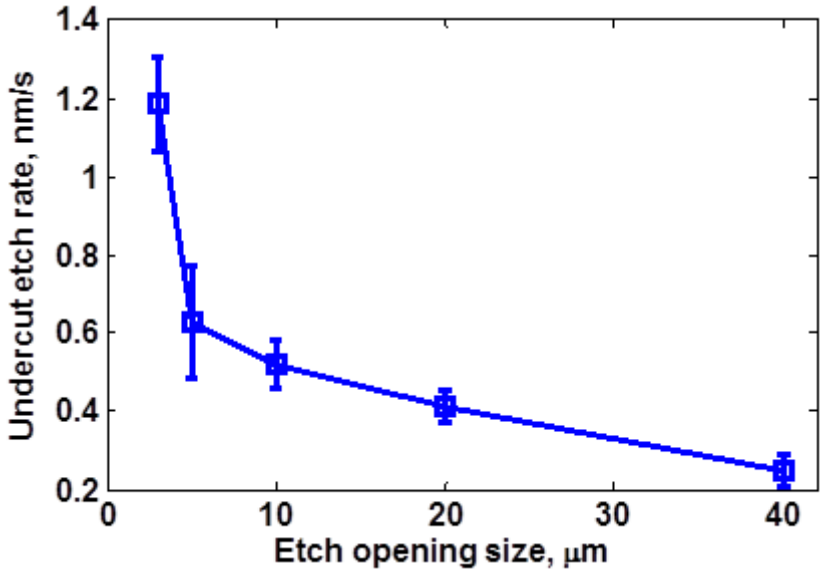
3.5.1.4 Dominance of loading effect over aperture effect

The undercut etch lengths for $3\ \mu m - 40\ \mu m$ of etch opening size have been measured at $105\ °C$ of substrate temperature and under constant $1000\ sccm/$ $100\ sccm$ of oxygen/nitrogen flow rates. Figure 3.14(a) shows the measured undercut etch length against the etch time. For all etch openings, the undercut etch length has been observed to increase linearly and then starts to saturate beyond $70\ minutes$ of etch time. This indicates the presence of diffusion limited etching beyond $70\ minutes$. After the relatively long time of etch release process, the diffusion of reactants has been reported to decrease and the etching rate reduced [34].

However, smaller etch openings have been observed to exhibit longer undercut etch length compared to the larger etch openings. These observations are indicative of the presence and dominance of the reaction-limited etching within the process [34][46][47].



(a) Measurement of the undercut etch length



(b) Measurement of the undercut etch rate

Figure 3.14 *(a) The saturation of undercut etch length after 70 minutes of etch time and (b) the decrease of undercut etch rate as the etch opening size increases.*

Figure 3.14(b) shows the undercut etch rate of the photoresist etch channels as a function of the etch opening size at $105\,°C$. The etch rate decreases as the etch opening increases, suggesting the presence of loading effect within the etch channel, which has been observed previously for the etch release process performed at low substrate temperature. In this case, other than low substrate temperature, the net loss

of reactive atomic oxygen/nitrogen species might have also been contributed from the increase of the photoresist area which is available to react with the atomic oxygen/nitrogen [46]. The absence of an increase in etch rate with respect to the increase in etch opening size is indicative of the absence of the aperture effect within the temperature regime studied [44][49].

3.5.2 Polyimide sacrificial layer etch release

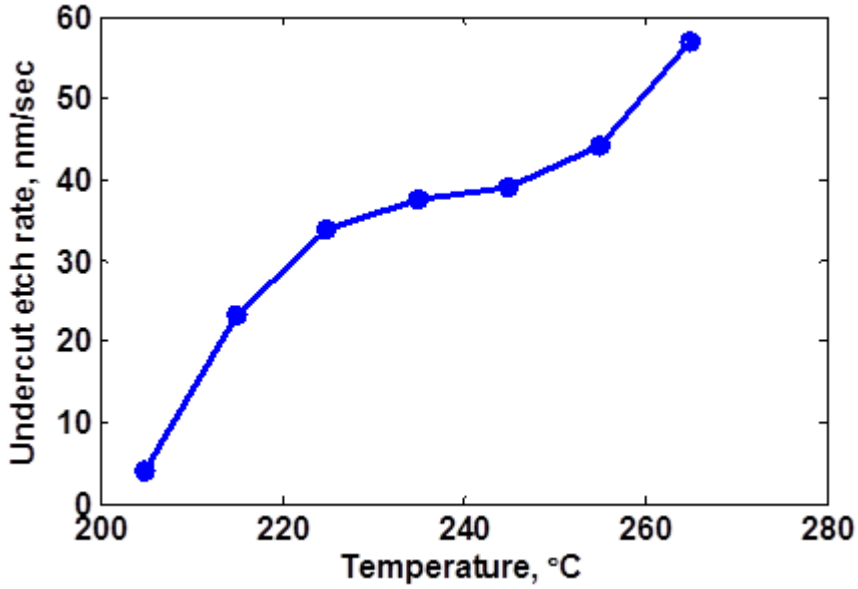
Polyimide has been considered for the characterisation of the sacrificial layer etch release process using the downstream oxygen/nitrogen plasma tool. For the fabrication of polyimide etch channels, 1.7 μm thickness of polyimide has been deposited, patterned and cured at 200 $°C$ for 30 $minutes$. Silicon dioxide of 1 μm thickness has been used as the transparent mask. Polyimide etch channels with 3 μm − 100 μm of etch openings have been fabricated.

3.5.2.1 Influence of substrate temperature on etch rate

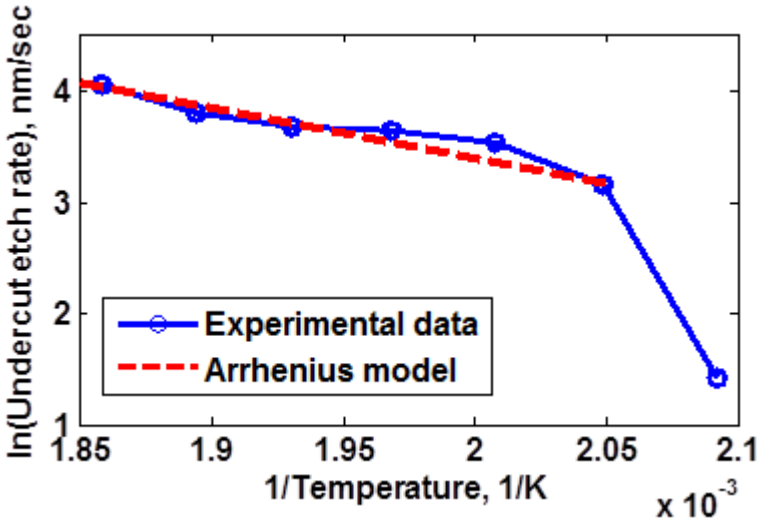
The polyimide etch release experiment has been conducted within the substrate temperature range of 205 $°C$ − 265 $°C$ [Figure 3.15(a)]. 3 μm of polyimide etch channel width and 2000 sccm/100 sccm of oxygen/nitrogen gas flow rates have been used. Similar to photoresist, the undercut etch rate for polyimide is seen to increase as a function of temperature. The temperature regime and oxygen flow rate are higher in the polyimide etch release experiment compared to photoresist, which results in higher etch rates measured for polyimide. No loading effect has been observed for 3 μm of polyimide etch channel width.

A fitted Arrhenius plot of polyimide's etch rate [Figure 3.15(b)] for temperatures above 210 $°C$ has been performed and the activation energy has been measured to be $E_a = 33.26\ kJ/mol$. The lowest temperature data point has been considered as an outlier for the fitted line since significant polyimide etching has been observed to start at substrate temperatures of higher than 210 $°C$. Below 210 $°C$, the etching rate tends to zero or no etching at all has been observed. T. H. Lin *et al* have reported on higher activation energy for polyimide, $E_a = 45.6\ kJ/mol$. In their work, the

polyimide has been cured at higher temperature ($250\,°C$) and longer time ($2.5\,hours$) compared to our process [40]. In addition, our substrate temperatures for the etch release process are higher.



(a) Measured undercut etch rate with respect to temperature



(b) Fitting of linear Arrhenius model into measurement data

Figure 3.15 *(a) Measurement of the increase in undercut etch rate for polyimide as the substrate temperature increases with* $3\,\mu m$ *of polyimide etch opening and* $2000\,sccm/100\,sccm$ *of oxygen/nitrogen. (b) The corresponding Arrhenius plot from the measurement data in (a) is fitted to the linear Arrhenius model.*

3.5.2.2 Influence of oxygen flow rate and etch opening size on etch rate and etch profile

At 245 $°C$, the undercut etch rate and the approximate etch profile for polyimide etch channels as a function of etch opening size and oxygen flow rate are shown in Figure 3.16. For all etch opening sizes, the undercut etch rate has been measured to increase with respect to the increase of oxygen gas flow rate, most likely due to the 1) increase in the reactive atomic oxygen density [35] or 2) more effective transport of the reactive atomic oxygen from plasma unit towards the chamber unit [40].

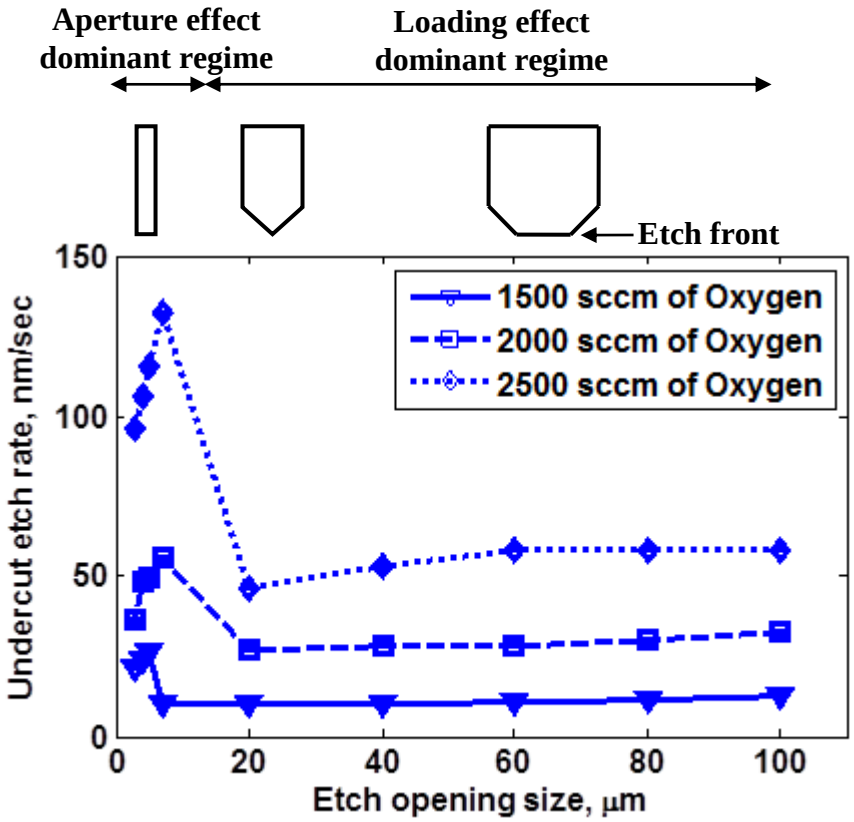


Figure 3.16 *Undercut etch rate and etch front profiles of the polyimide etch channels against the etch opening size with a variation of oxygen flow rates.*

For all oxygen flow rates in Figure 3.16, the etch rates are seen to reach maximum and then decrease to certain saturation values with respect to the increase in etch opening size. For 2000 $sccm$ and 2500 $sccm$ of oxygen flow rates, the undercut

etch rates saturate at $20\ \mu m$ of etch opening size, while for $1500\ sccm$ of oxygen flow rate, the saturation happens at $7\ \mu m$. Before reaching the maximum etch rate, the increase in etch rate with respect to the increase in etch opening size can be attributed to the aperture effect. A bigger etch opening size allows more oxygen to enter towards the etch channel and thus increases the etching rate of polyimide [44].

After the etch rate reaches a maximum, it decreases dramatically and reaches a saturation value. This observation indicates the presence of loading effect within the etch channel. The etch front illustrations for polyimide etch channels with respect to the increase in etch opening size are depicted in Figure 3.16. When the etch rate saturates, the etch front exhibits the profile characterised by the loading effect, which has been observed previously in Figure 3.12(a) for photoresist. Loading effect is caused by the loss of reactive atomic oxygen species. As the polyimide area increases with the increase of etch opening size, the net loss of reactive atomic oxygen increases and thus decreases the etching rate of polyimide. The loading effect dominant regime and aperture effect dominant regime for the polyimide etch release process are shown in Figure 3.16.

3.5.2.3 Influence of nitrogen flow rate on etch rate

The influence of nitrogen gas flow rate on the undercut etch rate of polyimide etch channels has been studied. At $2500\ sccm$ of oxygen flow rate, etch openings of $4\ \mu m$ from the aperture effect dominant regime and $100\ \mu m$ from the loading effect dominant regime have been considered. Figure 3.17 shows the increase in the undercut etch rate measured for both etch openings as the nitrogen gas flow rate increases.

S. Dzioba *et al* and J. M. Cook *et al* have reported on the concentration decay of the emanated reactive atomic oxygen species from the plasma unit due to the recombination mechanism [32][42]. Thus, nitrogen has been added to prevent the recombination of reactive atomic oxygen when the species are being extracted downstream towards the chamber unit. Nitrogen could also increase the concentration of reactive atomic oxygen in the plasma by the additional dissociation

and charge exchange mechanisms with the molecular oxygen, NO_2 and NO as shown in equation 3.3 - equation 3.5 [35][37][41][39]. Therefore, as the added nitrogen gas into the oxygen gas increases, the amount of reactive atomic oxygen would increase and this increases the etching rate of polyimide [36][37]. In addition, the reactive atomic nitrogen itself has been reported to be able to etch the polyimide [40][42].

$$N + O_2 \rightarrow NO + O \tag{3.3}$$

$$N + NO_2 \rightarrow N_2O + O \tag{3.4}$$

$$N + NO \rightarrow N_2 + O \tag{3.5}$$

In conclusion, the increase in nitrogen gas flow rate might serve to 1) increase the degree of molecular oxygen dissociation and 2) prevent the recombination of reactive atomic oxygen, hence increases the density of the atomic oxygen available to react with polyimide [35]; and 3) to increase the density of the reactive atomic nitrogen in the plasma to etch the polyimide [40].

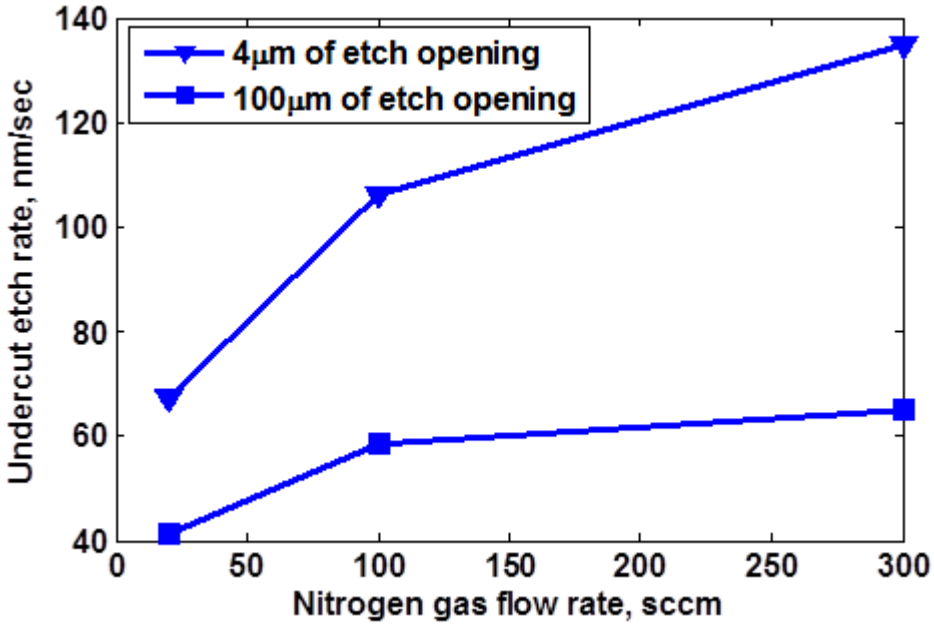


Figure 3.17 *Undercut etch rate increases as the nitrogen gas flow rate increases for 4 μm of etch opening (aperture effect dominant regime) and 100 μm of etch opening (loading effect dominant regime).*

3.6 Mechanical actuation and characterisation of aluminium bridges

The fabricated aluminium bridges have been actuated mechanically using a piezoelectric disc under vacuum condition. As the applied peak to peak voltage across the disc increases, the transferred vibration force from piezoelectric disc to the bridges increases. The amplitude and frequency of bridge vibration have been measured with Polytec OFV-5000 laser vibrometer.

For aluminium bridge width of smaller than 10 μm, the bridge vibration could not be detected using the laser. This is probably due to the size of laser beam spot which is larger compared to the bridge width. Thus, aluminium bridges with width bigger than 10 μm have been chosen for the measurement. However, since the aluminium bridges of length 0.57 $mm - 1.62\ mm$ sagged down and touched the substrate as the bridge width becomes bigger than 10 μm, the frequency measurement for aluminium bridges of 0.57 $mm - 1.62\ mm$ length could not be executed.

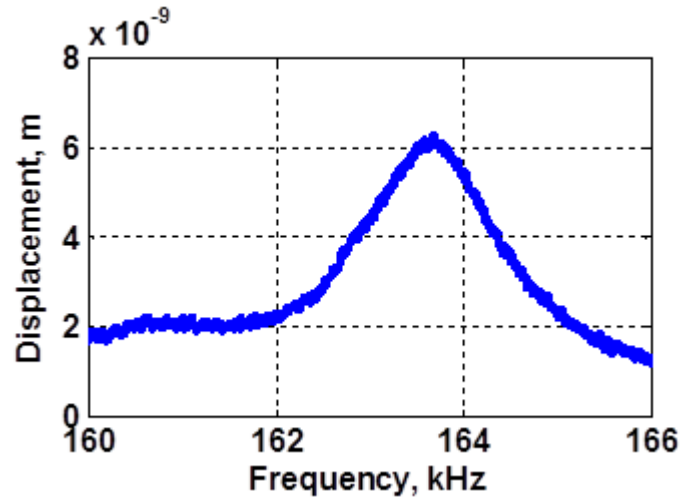
Label	$B11$	$B12$
Length, l_b	278 μm	92 μm
Thickness, t_b	0.5 μm	0.5 μm
Width, w_b	15 μm	15 μm

Table 3.1 *Geometrical dimensions for the aluminium bridges labelled as $B11$ and $B12$.*

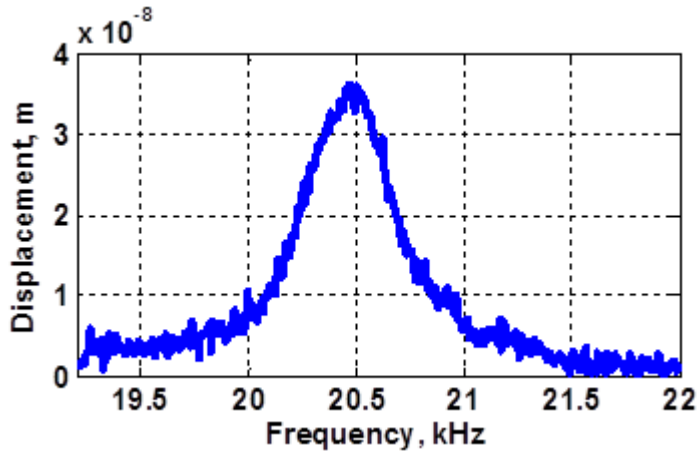
Therefore, two aluminium bridges have been considered, $B11$ and $B12$ with the geometrical dimensions described in Table 3.1. These bridges are shorter than 0.57 mm and wider than 10 μm. Thus, the fabricated aluminium bridges $B11$ and $B12$ are free-standing and the corresponding bridge vibration is able to be detected by the laser. The expected resonant frequency f_1 for $B11$ and $B12$ have been calculated from equation 2.21 to be 33.86 kHz and 310 kHz respectively, assuming the bulk values of $E = 70\ GPa$ and $\rho = 2700\ kg/m^3$.

3.6.2 Compressive stress-induced bridges

The measured frequency responses for $B11$ and $B12$ from the laser vibrometer are shown in Figure 3.18.



(a) $B12$



(b) $B11$

Figure 3.18 *The measured frequency responses from the aluminium bridges labelled as (a) $B12$ of length $l_b = 92\ \mu m$ and (b) $B11$ of length $l_b = 278\ \mu m$.*

In Figure 3.18(a), the measured resonant frequency for $B12$ is $f_1 \sim 163.7\ kHz$ with $\sim 6\ nm$ of vibration displacement and a quality factor of $Q_{10} \sim 40$. The measured resonant frequency is approximately two times smaller than the calculated value $f_1 = 310\ kHz$. The finite element model for $B12$ has been created and the presence of biaxial residual stress within the aluminium bridge structure has been included in

the modal analysis. From the finite element model simulation, a biaxial residual compressive stress of $\sigma_{comp} = -9\ MPa$ within the aluminium layer has been found to change the resonant frequency of aluminium bridge $B12$ from $310\ kHz$ to $165\ kHz$.

As for the aluminium bridge $B11$, the measured resonant frequency is $f_1 \sim 20.5\ kHz$ with $\sim 36\ nm$ of vibration displacement and $Q_{10} \sim 22$ [Figure 3.18(b)]. The measured resonant frequency is approximately ~ 1.8 times smaller than the calculated value $f_1 = 33.86\ kHz$. From the finite element model simulation, the biaxial residual compressive stress of $\sigma_{comp} = -1\ MPa$ has been found to alter the resonant frequency of aluminium bridge $B11$ from $33.86\ kHz$ to $20\ kHz$.

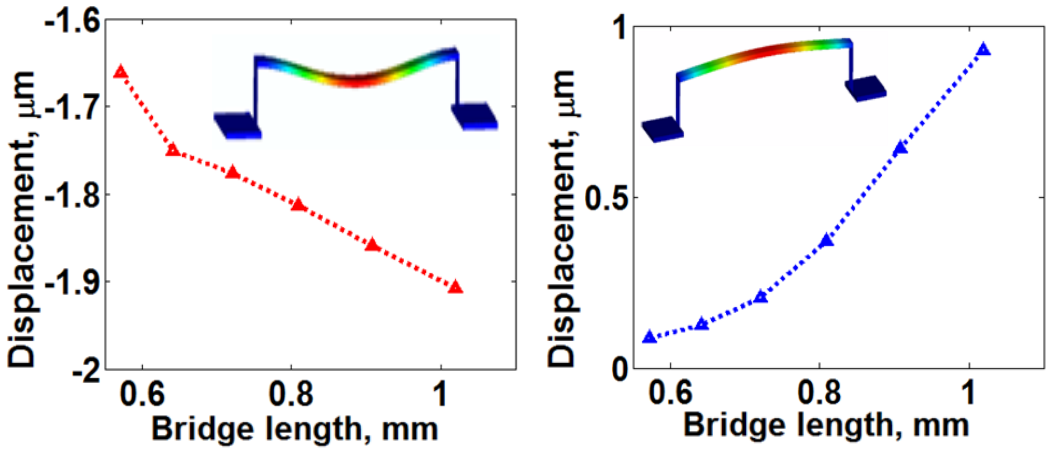
The aluminium bridges have been actuated mechanically in vacuum medium, making the quality factor of the bridges to be higher than the desired $Q_{10} = 0.6 - 10$ from the cochlear response. In addition, the mechanical input force onto the aluminium bridge $B11$ has been increased by increasing the applied AC voltage across the piezoelectric disc. The vibration displacement increases from $36\ nm$ to $130\ nm$ as the applied AC voltage increases from $5\ V$ to $8\ V$. Thus, the mechanical sensitivity for aluminium bridge $B11$ is $\sim 31\ nm/V$.

The deviation of the frequency measurements from the theoretical predictions and the finite element model simulation results have indicated that the fabricated aluminium bridges of length $0.092\ mm - 0.278\ mm$ are under a certain value of compressive stress which has been found to be dependent on the size of the bridge structure. The shorter bridge, $B12$ has been simulated to have higher compressive stress compared to the longer one, $B11$. Overall, the biaxial residual compressive stress within the aluminium bridge has been extracted to decrease from $-9\ MPa$ to $-1\ MPa$ as the bridge length increases from $0.092\ mm$ to $0.278\ mm$.

3.6.3 Influence of stress and bridge length on bridge deflection

As the bridge length becomes longer than $0.278\ mm$, whether the compressive stress within the structure would reduce further and evolve into tensile stress is unknown.

However, from the finite element model simulation, the presence of tensile stress within the bridge has been found to cause the sagging of the aluminium bridge structure. In Figure 3.19, the displacement of aluminium bridge deflection due to the presence of tensile or compressive stress within the structure has been simulated. The simulation has been performed with the aluminium bridge length increases from 0.57 mm to 1 mm and at a constant bridge width of $w_b = 15\ \mu m$. In the simulation, the biaxial residual tensile and compressive stresses within the aluminium bridge layer have been assumed to be constant with respect to the bridge length.



(a) Bridge under tensile stress **(b)** Bridge under compressive stress

Figure 3.19 *The aluminium bridges have been simulated to deflect (a) downwards due to the presence of tensile stress and (b) upwards due to the presence of compressive stress within the bridge. The displacement of aluminium bridge deflection increases with respect to the increase in bridge length.*

In Figure 3.19(a), the aluminium bridges under tensile stress have been simulated to deflect downwards giving negative displacement values. The increase in bridge length has been seen to increase the displacement of downwards deflection. The simulation results might explain the collapsing of the fabricated aluminium bridge structures when the bridge length increases and postulate that the sagged aluminium bridges are under the influence of tensile stress. On the other hand, the compressive stress within the aluminium bridge layer has caused the bridge to deflect upwards

giving positive displacement values and the buckling increases with the increase in bridge length [Figure 3.19(b)].

The properties of the material used for the bridge structure are the essential factors that determine the reliability of the bridge's mechanical performance. As the bridge length increases, the aluminium metal layer might not be able to withstand the tensile stress within the structure, causing it to deform. In order to avoid the bridge from collapsing onto the substrate, the chosen metal for the bridge should have a considerably small compressive/tensile stress and/or possess high yield strength and Young's modulus to withstand the stress. Tantalum with higher yield strength and Young's modulus compared to aluminium will be considered in Chapter 4.

3.7 Conclusion

In this chapter, the fabrication process for creating the bridge of RGT has been proposed. The selective sacrificial layer etch release scheme has been employed. The process involves the etch release of aluminium bridge structure from the photoresist sacrificial layer using the reactive atomic oxygen and nitrogen as the etchants. The photoresist sacrificial layer has to be baked on a hotplate as the trapped moisture within the layer would afterwards cause a distortion of the bridge structure. The released aluminium bridges of width $< 10\ \mu m$ and length $< 1\ mm$ have been observed to be free-standing with clean surfaces. On the other hand, the fabricated aluminium bridges of length $0.57\ mm - 1.62\ mm$ and width $> 10\ \mu m$ have been found to sag down and touch the substrate. Thus, in order to fabricate a free-standing aluminium bridge structure which has been sputter-deposited from the Balzers, the limits of width and length for the bridge are $w_b < 10\ \mu m$ and $l_b < 1\ mm$, respectively.

The developed downstream isotropic dry-etch release technique using the reactive atomic oxygen and nitrogen species in the oxygen/nitrogen plasma tool has been found to be capable of releasing the aluminium bridge structures and provide a fast, clean and damage-free etch release process. The photoresist and polyimide

sacrificial layer etch release process in the downstream oxygen/nitrogen plasma tool has been characterised. The test structures which consist of the photoresist and polyimide etch channels with different etch opening sizes have been fabricated and tested. For both sacrificial layers, the increase in substrate temperature during etch release has been found to increase rate of the etching process significantly. The activation energies have been measured to be $E_a = 45.31\ kJ/mol$ for photoresist and $E_a = 33.26\ kJ/mol$ for polyimide, which agree fairly well with the measured activation energies from others. For photoresist, the loading effect has been found to be dominant at substrate temperatures of $< 125\ °C$ while for polyimide, there has been a transition of aperture effect at small etch openings to loading effect at wider etch openings for substrate temperature of $245\ °C$. In addition, the increase in oxygen and nitrogen gas flow rates in the oxygen/nitrogen plasma has been shown to increase the etching rate of polyimide. The etch release process for releasing the aluminium bridge structures from the photoresist sacrificial layer has been optimised to high substrate temperature of $250\ °C$ and considerably high oxygen/nitrogen gas flow rates of $2500\ sccm/500\ sccm$.

After the successful fabrication of the aluminium bridges, mechanical actuations have been performed to measure the bridges' frequency responses. Due to the limitation of the laser vibrometer, the frequency measurement for the free-standing aluminium bridges of width $< 10\ \mu m$ and length $0.57\ mm - 1\ mm$ could not be executed. Thus, aluminium bridges of width $> 10\ \mu m$ and length $0.092\ mm - 0.278\ mm$ have been fabricated and measured. The measured resonant frequencies have been found to be approximately twice smaller than the theoretical predictions, suggesting that the aluminium bridges are under the influence of biaxial residual compressive stress. From finite element model of the aluminium bridges, the biaxial residual compressive stress within the structures has been extracted to decrease from $-9\ MPa$ to $-1\ MPa$ as the bridge length increases from $0.092\ mm$ to $0.278\ mm$.

From the finite element model of the aluminium bridges with length $> 0.57\ mm$, the biaxial residual tensile stress within the structures has been simulated to cause the

bridges to deflect downwards. In addition, the downwards displacement of the bridge deflection increases with the increase in bridge length. The presence of biaxial residual tensile stress within the aluminium bridges might explain the collapsing of the fabricated aluminium bridge structures as the bridge length increases. The developed etch release technique is believed to be gentle enough to release the aluminium bridge structures, leaving an assumption that the failure of having free-standing aluminium bridges of length $> 1\,mm$ might come from the limitation of the metal layer itself. The properties of the metal used for the bridge structure i.e. stress, Young' modulus will determine its mechanical performance. In Chapter 4, tantalum metal with better mechanical properties has been used to replace aluminium.

Chapter 4: Fabrication process and mechanical characterisation of tantalum bridges

4.1 Introduction

In this chapter, the second iteration for the fabrication of RGT bridge structure will be carried out. In Chapter 3, a reliable etch release process has been developed to release the aluminium bridge structure from the photoresist sacrificial layer. The sagging issue of the aluminium bridge with length $> 1\ mm$ has led to the search for a new bridge material. In this chapter, the material for the bridge structure will be changed from aluminium to tantalum. The fabrication process of the tantalum bridge structure will be described and the developed downstream oxygen/nitrogen plasma etch release technique will be employed to release the tantalum bridge from the photoresist sacrificial layer. The designed tantalum bridge length for $B1 - B10$ and $C1 - C10$ described in Table 2.2 in Chapter 2 will be used in the fabrication. The profile of the released tantalum bridges will be studied and the frequency response will be measured in air and vacuum medium.

In many cases, MEMS bridges have been employed as the test structures to characterise the properties of the material used. The measurement of pull-in voltage [70], resonant frequency [67] or physical deformation [71][75] of the bridge have been reported and models have been incorporated with the measurement results in order to extract stress or Young's modulus of the material used. In our study, straight and buckled tantalum bridges have been fabricated. The stress within the tantalum bridge structures for both straight and buckled cases will be characterised

by measuring the resonant frequency and physical deflection of the fabricated bridges, respectively.

In straight tantalum bridge case, the residual stress within the tantalum structures will be extracted by fitting the measured first three modal frequencies to their analytical frequency model. Finite element model (FEM) will be created and modal analysis will be conducted in order to verify the extracted residual stress and to examine the modal behaviour of the straight bridges. In buckled tantalum bridge case, the maximum vertical deflection of the bridge will be measured and fitted to the static buckling model of the tantalum bridge structure to extract the residual stress. Then, the extracted residual stress will be validated from the finite element model and the modal shapes of the buckled tantalum structures will be simulated as well.

4.2 Fabrication of tantalum bridges

In the second iteration, tantalum has been proposed to replace aluminium for the fabrication of the bridge structure due to its higher yield strength ($\sim$10 times higher) and Young's modulus ($\sim$2.5 times higher) compared to aluminium [53]-[57]. Thus, the fabricated tantalum bridge structure will appear stronger physically, preventing it from collapsing to the substrate as has been seen previously from the fabricated aluminium bridges. In addition, tantalum is one of the refractory metals that possesses excellent chemical and wear resistance with high melting point of 3000 ℃ [50][59][60]. Tantalum films have been used as the protective coatings on surfaces that are subjected to high stresses and harsh environments [61][62]. In section 2.6.2.1, the tantalum bridges have been calculated to have lower resonant frequencies compared to the aluminium bridges of the same dimensions as the ratio of Young's modulus to mass density for tantalum is approximately twice smaller than aluminium's [55]-[58].

4.2.1 Deposition and etching of tantalum

The fabrication steps for creating the tantalum bridges are similar with the process steps that have been used to fabricate the aluminium bridges, described in section

3.3. A 3-inch silicon wafer with thermally grown silicon dioxide layer is used as the substrate. SPR 220-4.5 photoresist of $\sim 4.4\ \mu m$ thickness is employed as the sacrificial layer. The photoresist sacrificial layer has been deposited and patterned photolithographically to define the bridges' anchor regions. Then, the photoresist sacrificial layer has been baked on the hotplate at $135\ °C$ in order to vaporise out all solvents from the sacrificial layer, before being sputter-deposited with tantalum. Unlike aluminium, the tantalum sputter-deposition process has been observed to cause the photoresist sacrificial layer to reflow. Temperature of higher than $135\ °C$ during the tantalum sputter-deposition process has been suspected to have caused the photoresist to liquefy. The heat can come from the exposure of plasma discharge and/or from the kinetic energy of the sputtered energetic particles onto the photoresist sacrificial layer [61]. The physical appearance of the deposited tantalum layer on top of the photoresist sacrificial layer degrades badly as the photoresist liquefies. Thus, the photoresist sacrificial layer has been baked at $200\ °C$ and no observable defects have been detected from the deposited tantalum layer afterwards. The measured photoresist sacrificial layer thickness after the baking step is $\sim 3.4\ \mu m$.

The tantalum has been sputter-deposited on top of the photoresist sacrificial layer using DC magnetron sputtering system called OPT Plasmalab 400 sputter tool at $500\ W$ and $3\ mTorr$ of argon gas pressure, giving a deposition rate of $3\ nm/min$. A duration of $166\ minutes$ for the sputter-deposition process is required to achieve $0.5\ \mu m$ thickness of tantalum layer. Thereafter, SPR350 Shipley photoresist of $1.6\ \mu m$ thickness has been deposited and patterned with UV lithography to define the outline of the bridge structures on the tantalum layer. Then, the tantalum is etched to form the bridge structure using the reactive ion etching (RIE) technique that employs $SiCl_4$/Ar plasma as the etching gases. The etch rate for tantalum is $4\ nm/min$, much smaller than the etch rate for aluminium ($25\ nm/min$). A total etching time of $\sim 2\ hours$ to pattern the tantalum bridges will harden the top photoresist mask that is exposed to the RIE plasma for such long period of time. Thus, a longer ashing process in the barrel asher ($15\ minutes$) is required to remove the top photoresist mask. After dicing the 3-inch wafer into $1\ cm \times 1\ cm$ chips, the tantalum bridge

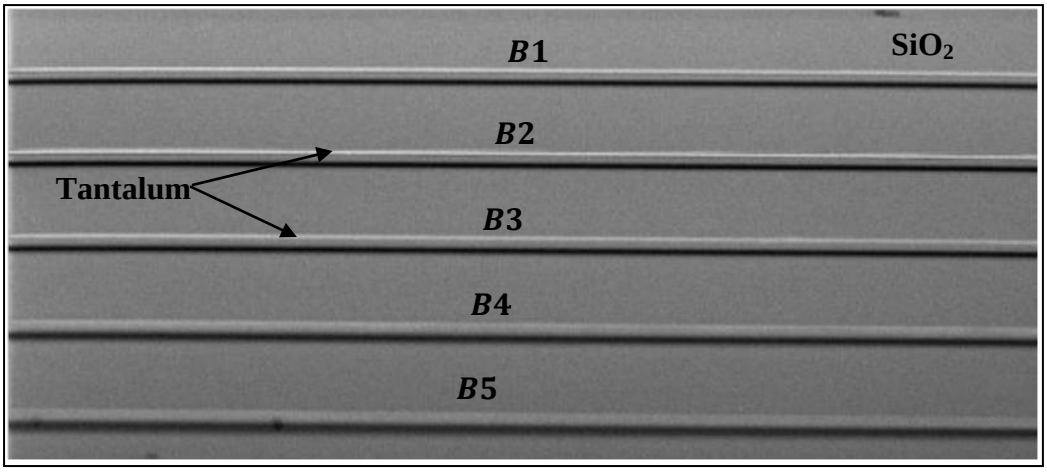
structures have been released in the downstream oxygen/nitrogen plasma tool with an etch rate of $22\,nm/sec$, under the etch release conditions of $250\,°C$ substrate temperature and $2500\ sccm/500\ sccm$ oxygen/nitrogen gas flow rates.

4.2.2 Straight and buckled tantalum bridges

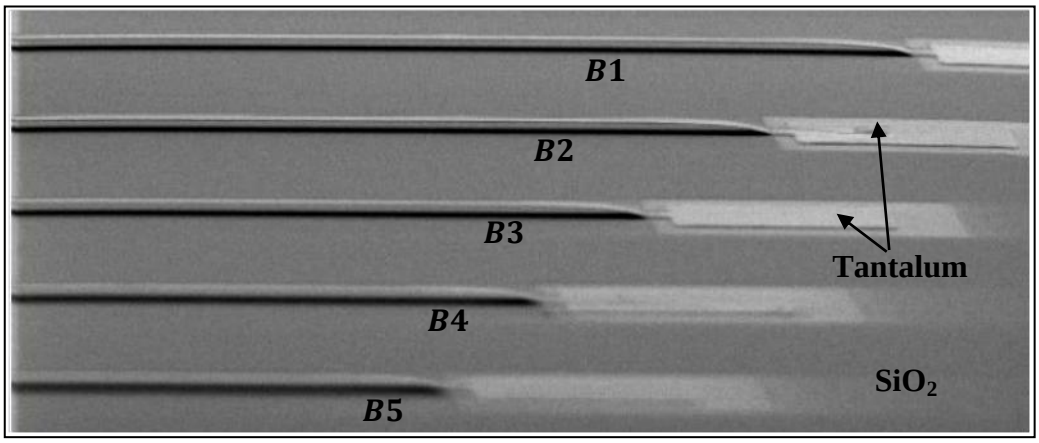
The tantalum bridges with bridge length of $l_b = 0.57\,mm - 5.8\,mm$ and bridge width of $w_b = 10\,\mu m - 30\,\mu m$ have been fabricated. The majority of the released structures have been observed to be free-standing and do not collapse onto the substrate. The released tantalum bridges possess either the straight or buckle profile. An array of five straight tantalum bridges, labelled as $B1 - B5$ of length $l_b = 1.62\,mm - 1\,mm$ which has been released from $3.4\,\mu m$ of photoresist sacrificial layer is depicted in Figure 4.1. From the scanning electron microscopy (SEM) images, each of the fabricated tantalum bridges is seen to be free-standing with uniform straight profile and without noticeable deformation along the bridge length. The dark lines that appear underneath the bridges are the bridge shadows.

In Figure 4.2, two arrays of buckled tantalum bridges labelled as $B1 - B10$ and $C1 - C10$ have been released from the photoresist sacrificial layer of $3.4\,\mu m$ thickness. The range of bridge length for $B1 - B10$ [Figure 4.2(a)] and $C1 - C10$ [Figure 4.2(b)] are $l_b = 1.62\,mm - 0.57\,mm$ and $l_b = 5.8\,mm - 1.8\,mm$, respectively. The released tantalum bridges have been observed to deform and deflect upwards, creating the arched/curved bridge shapes. From the SEM images, the maximum vertical deflection at the centre of the tantalum bridge has been observed to increase as the length of the bridge increases.

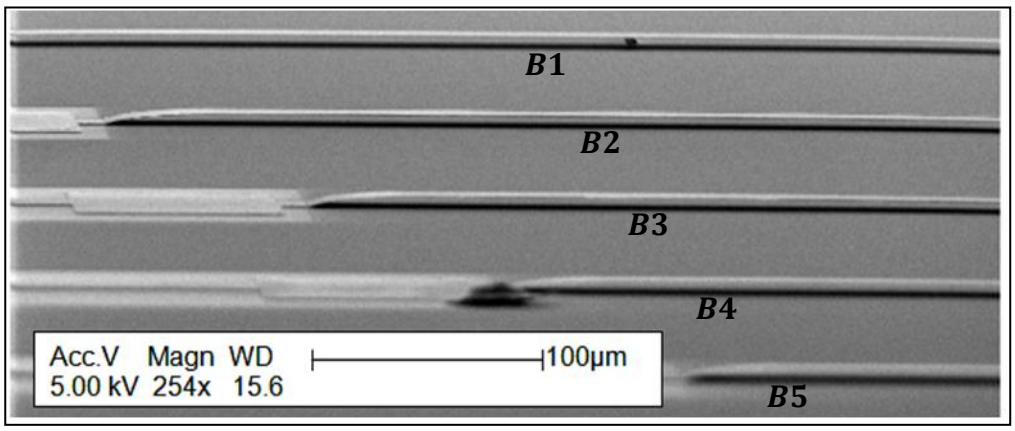
The observed outcomes from the fabricated tantalum bridges indicate that the tantalum might be a better material than aluminium for the fabrication of the free-standing and practically long bridge structures for the RGTs. The tantalum bridges might be stronger than the aluminium bridges as the tantalum film layer has been reported to possess higher yield strength and Young's modulus [53]-[57]. However, the profile of the fabricated tantalum bridges has been found to be inconsistent as the released structures demonstrated either a straight or buckle behaviour.



(a) $B1 - B5$ at the middle region of the bridges

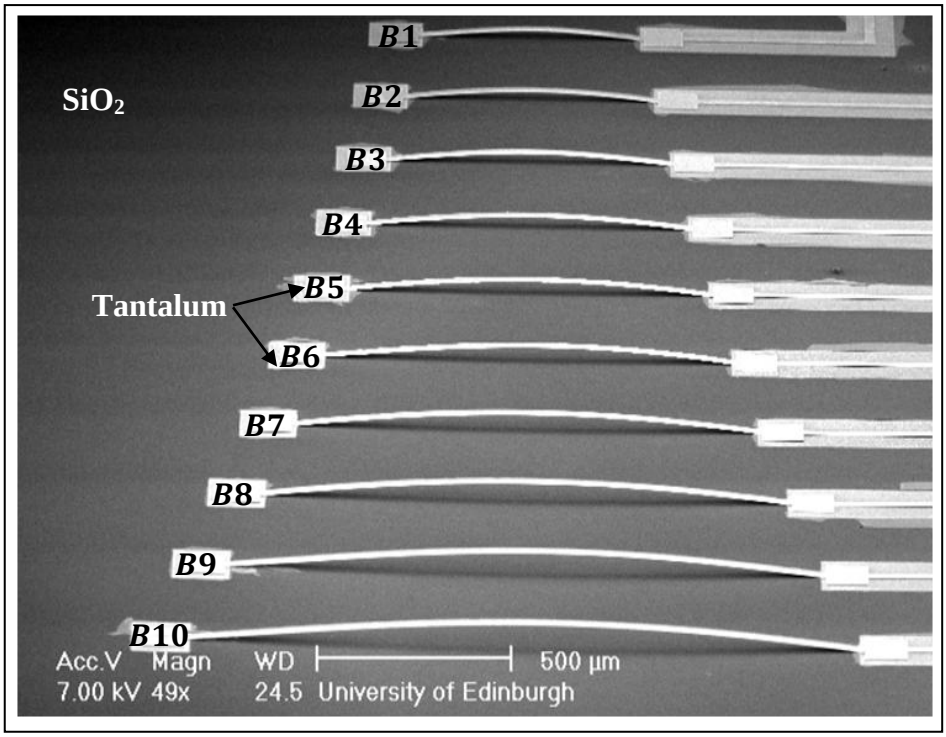


(b) $B1 - B5$ at the anchor region of the bridges

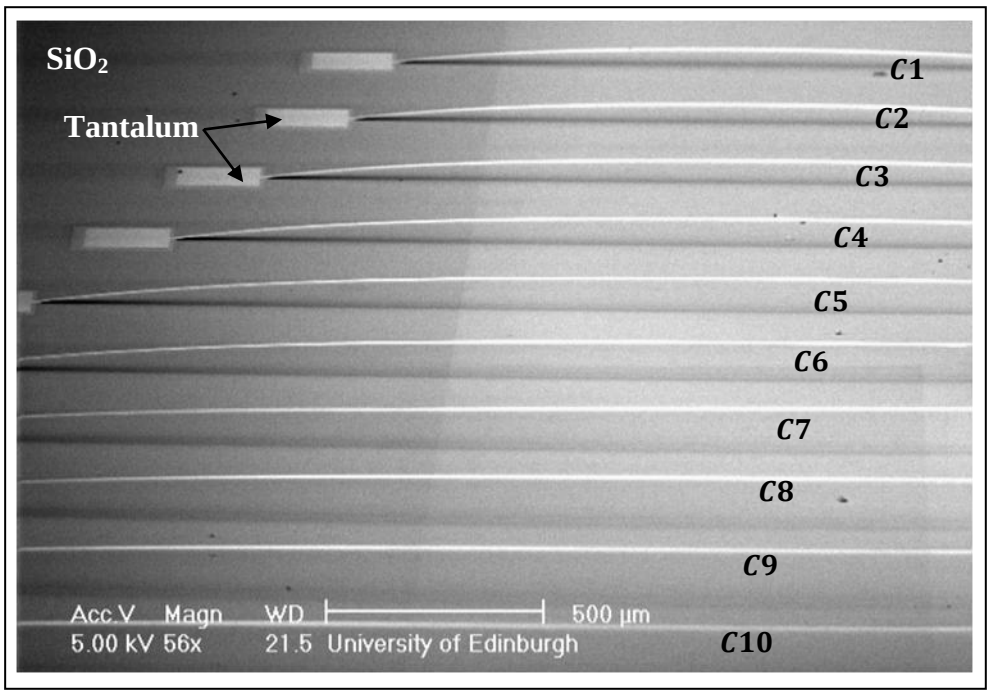


(c) $B1 - B5$ at the anchor region of the bridges

Figure 4.1 *(a)-(c) The SEM micrograph images of the released straight tantalum bridges* $B1 - B5$ *with bridge length of* $l_b = 1.62\ mm - 1\ mm$. *The bridge width has been measured to be* $w_b \sim 25\ \mu m$ *with thickness of* $t_b \sim 0.5\ \mu m$ *and the distance from bridge to substrate is* $d_i \sim 3.4\ \mu m$.



(a) $B1 - B10$ tantalum bridges



(b) $C1 - C10$ tantalum bridges

Figure 4.2 *The SEM micrograph images of the released buckled tantalum bridges with* $w_b \sim 30\,\mu m$, $t_b \sim 0.5\,\mu m$ *and (a)* $l_b = 1.62mm - 0.57\,mm$ *for* $B1 - B10$ *(b)* $l_b = 5.8\,mm - 1.8\,mm$ *for* $C1 - C10$.

In both cases, the tantalum has been sputter-deposited from the same OPT tool with similar sputter-deposition parameters. The subsequent processing steps to fabricate the bridge structure from the sputter-deposited tantalum metal layer might have influenced the bridge's profile. The source of the inconsistency could not be identified, but the material properties and microstructures of the sputter-deposited tantalum film layer have been postulated to be different in each case.

The finite element model simulation for aluminium bridge structures in section 3.6.3 have shown that, for the case when the bridges are deflected upwards (downwards), the exhibited stress within the bridges is compressive (tensile). In addition, small values of compressive or tensile stress within the bridges have been simulated to produce insignificant deflection along the bridge length i.e. straight bridges. Therefore, other than the influence of yield strength and Young's modulus of the material structure, the existence of stress within the tantalum bridge might as well have assisted the bridge to be free-standing and more importantly, influenced the shape of the fabricated bridges. The stress analyses for the straight and buckled tantalum bridges are treated separately and their corresponding mechanical frequency responses have been characterised.

4.3 Characterisation of straight tantalum bridges

In this section, the biaxial residual stress within the straight tantalum bridges has been found to be tensile. The first three modal frequencies of the bridges have been measured and compared with the analytical frequency model of the tensile-stressed bridges. The biaxial residual tensile stress values have been extracted by fitting the measured frequencies into the analytical model using the least mean squares method.

In addition, the quality factor and vibration displacement of the fabricated straight $B1 - B10$ tantalum bridges have been measured. Using the measured mechanical responses of the fabricated straight tantalum bridges, the expected RGT electrical output responses have been estimated from the mathematical model of RGT described in Chapter 2.

4.3.1 Tensile stress-induced bridges

The fabricated straight tantalum bridges $B1 - B10$ on $1\ cm \times 1\ cm$ chip have been actuated mechanically and the frequency responses of the bridges have been measured in vacuum using Polytec OFV-5000 laser vibrometer. In mechanical actuation, the chip has been mounted on a piezoelectric disc. The mechanical vibration has been induced by applying AC voltage across the piezoelectric disc and then the vibration is transferred to the bridges. The laser beam spot has been positioned at the middle region of the bridge length. More than one mode has been detected from the tantalum bridge structure.

In Figure 4.3, the detected resonant peaks for the tantalum bridge $B3$ of length $l_b = 1.28\ \mu m$ have been plotted. The first mode f_1 i.e. fundamental resonant frequency has been measured to be $5.5\ kHz$ followed by $11\ kHz$, $18\ kHz$ and $23\ kHz$ as the second f_2, third f_3 and fourth mode f_4. The symmetrical modes (first and third) have been observed to have higher displacement amplitudes compared to the antisymmetrical modes (second and fourth).

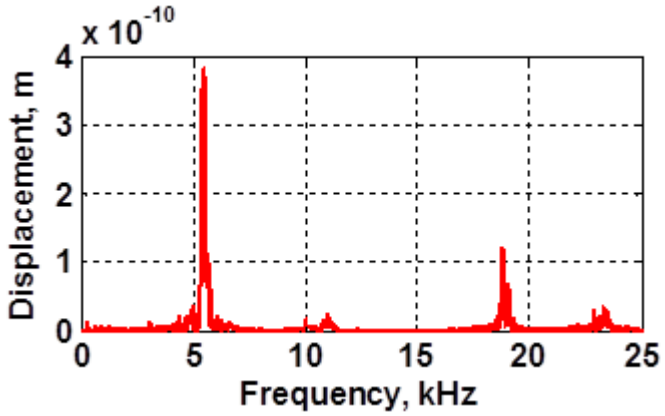


Figure 4.3 *Four modes have been detected from the measured frequency response of the straight tantalum bridge $B3$ with $l_b = 1.28\ \mu m$.*

Theoretically, Rayleigh has predicted the vibrational modal ratios of $1 : 2.7 : 5.4 : 8.9$ for a fixed-fixed bridge [21]. Thus, the predicted first four modes for bridge $B3$ should be $5.5\ kHz$, $15\ kHz$, $30\ kHz$ and $49\ kHz$ respectively. In our measurements however, higher modes have been found to be approximately the multiples of the

first mode which agree well with the vibrational modal ratios of a string instead of the fixed-fixed bridge [16].

A bridge structure has been reported to behave more like a string when its rigidity is much smaller than the exhibited biaxial residual tensile stress within the structure [16]. This indicates that the fabricated straight tantalum bridge structure is being subjected to the axial tensile force along the bridge length and behaves like a stretched wire/string. The residual tensile stress might have been induced within the fabricated tantalum bridge structure during the sputtering of tantalum layer onto the photoresist sacrificial layer and/or due to other subsequent processing steps. The origin of tensile stress within the sputter-deposited metal has been reported to be due to the grain boundary shrinkage which produce a metal film with columnar porosity microstructure [63][64].

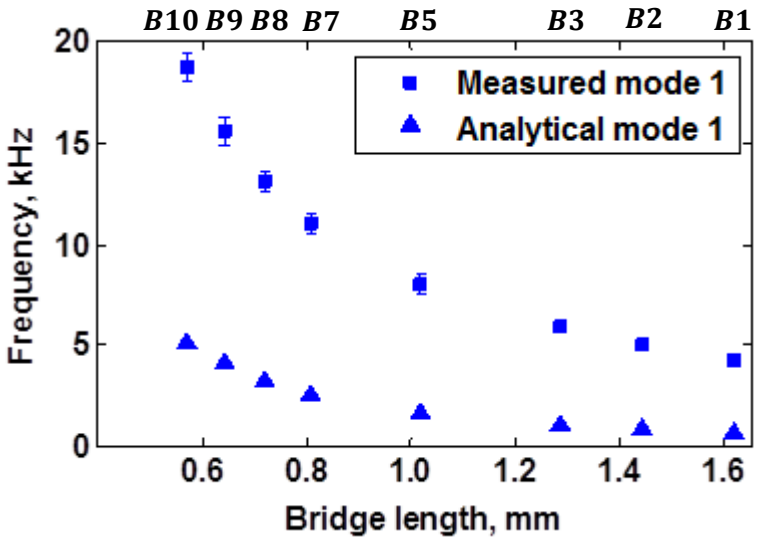


Figure 4.4 *The first modes for the straight tantalum bridges $B1 - B10$ of length $l_b = 1.62\,mm - 0.57\,mm$ are measured to be higher compared to the calculated analytical first modes of the unbuckled, stress-free tantalum bridges.*

The first mode f_1 for the straight tantalum bridges $B1 - B10$ ($B4$ and $B6$ are not available) have been measured to be $4.2\,kHz - 18.8\,kHz$ and plotted in Figure 4.4 with respect to the bridge length $l_b = 1.62\,mm - 0.57\,mm$. From equation 2.1, the first mode f_1 for the unbuckled, stress-free tantalum bridges $B1 - B10$ have been

calculated with respect to their length and compared with the measurement in Figure 4.4 [30][66]. E and ρ for tantalum have been assumed to be $175\,GPa$ and $16\,300\,kgm^{-3}$, respectively [56]. It can be seen that the measured first mode from each of the straight tantalum bridges is about four to six times higher than its stress-free analytical value. Thus, the presence of residual tensile stress within the fabricated tantalum bridge structure has the influence of increasing its resonant frequency. The magnitude of the induced biaxial residual tensile stress within the tantalum bridges can then be quantified by fitting the analytical frequency model of the tensile-stressed bridges to the measurement.

4.3.1.1 Tensile stress extraction

An ideal bridge can be regarded as a flat, homogeneous, prismatic beam with rigid supports at both ends. The analytical model for the n^{th} mode, $f_n(\sigma_{tens})$ of the transverse vibrating bridge that is being subjected to an axial tensile force, can be approximated as in equation 4.1 [30][66].

$$f_n(\sigma_{tens}) = f_n(0)\sqrt{(1 + \frac{\gamma_n(1-\nu)\sigma_{tens}A_b{l_b}^2}{12EI})} \tag{4.1}$$

$\upsilon = 0.34$ is the Poisson's ratio and σ_{tens} is the biaxial residual tensile stress of the tantalum bridge [65]. $f_n(0)$ is the n^{th} mode of the bridge without the influence of tensile stress and γ_n is the coefficient that relates the tensile stress to modal stiffness [66]. The values of γ_n for $n = 1, 2, 3$ have been calculated to be 0.2949, 0.1453 and 0.0812 respectively. A_b, l_b, E and I have been defined previously as the cross sectional area, length, Young's modulus and moment of inertia of the bridges.

In order to determine the value of tensile stress that exists within the fabricated straight tantalum bridges $B1 - B10$, the first three vibrational modes of the bridges have been measured. Then, equation 4.1 has been used to calculate the theoretical values of the first three modes i.e. $f_n(\sigma_{tens})$ for $n = 1 - 3$ using a range of stress values $\sigma_{tens} = 0\,MPa - 20\,MPa$ and Young's Modulus values $E = 100\,GPa - 200\,GPa$ for the range of bridge length $l_b = 0.57\,mm - 1.62\,mm$. Afterwards,

these calculated frequencies have been fitted to the measured first, second and third mode of the tantalum bridges $B1 - B10$ using the least mean squares method and the stress within the bridges at modes $n = 1 - 3$ have been extracted [67].

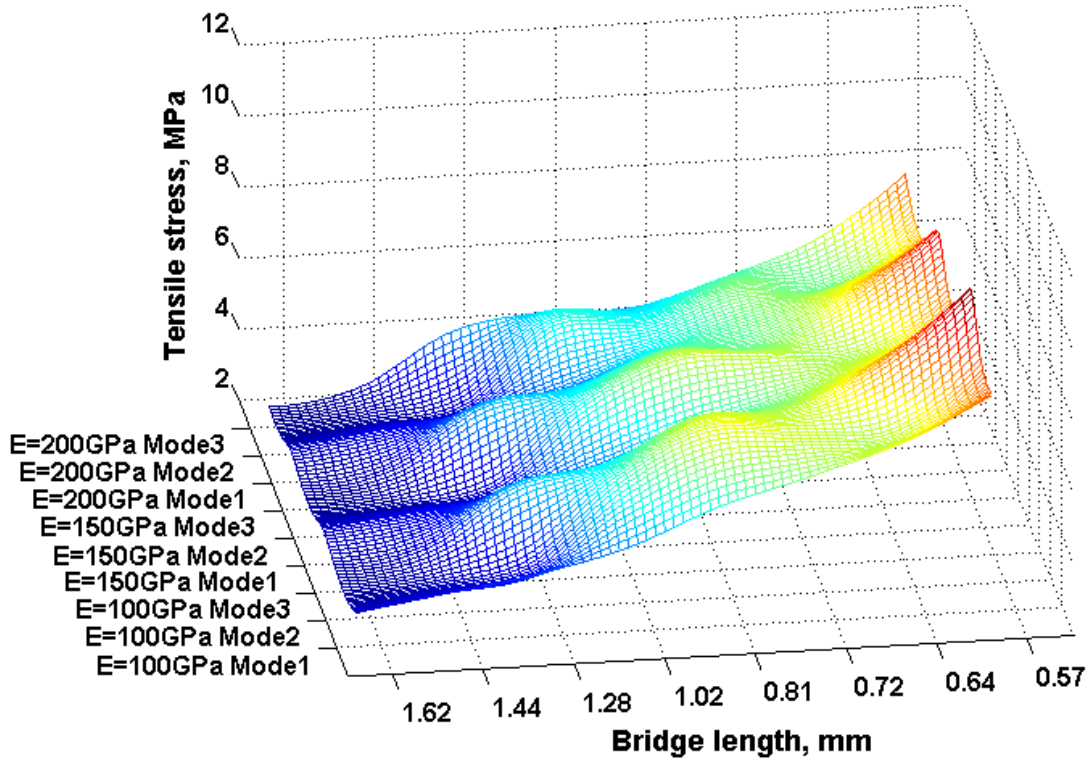


Figure 4.5 *The extracted biaxial residual tensile stress for the straight tantalum bridges increase with respect to the decrease in bridge length. Young's modulus of* $E = 100\ GPa - 200\ GPa$ *at mode* $n = 1 - 3$ *have been considered in the calculation.*

The extracted values of tensile stress for each tantalum bridge length are plotted in Figure 4.5 with $n = 1 - 3$ and $E = 100\ GPa - 200\ GPa$. The extracted tensile stress has been estimated to increase from $\sim 3\ MPa$ to $\sim 10\ MPa$ as the bridge length decreases from $1.62\ mm$ to $0.57\ mm$. In addition, the extracted stresses do not vary greatly with respect to the Young's modulus, $E = 100\ GPa - 200\ GPa$ and mode number, $n = 1 - 3$. From here onwards, the Young's modulus for the tantalum bridge will be assumed to be $E = 175\ GPa$ in our analysis [56] and the tensile stress for each tantalum bridge length will be taken as the average stress amongst the three modes.

The extracted residual tensile stresses of $\sim 3\,MPa - 10\,MPa$ from our straight tantalum bridges are comparable with the one measured by Iimura *et al* who have reported a total tensile stress of $30\,MPa$ for the sputter-deposited tantalum film layers of $0.7\,\mu m - 0.8\,\mu m$ thickness on a 3-inch wafer, using $2.2\,mTorr$ of xenon gas pressure [68]. In our process, a DC sputtering has been employed instead of RF sputtering with $3\,mTorr$ of argon gas pressure. The stress within the sputter-deposited tantalum film layer has been reported to be different under different deposition parameters [68]. This will be further discussed in section 4.4.1.

4.3.1.2 Tensile stress validation

The finite element models for the straight tantalum bridges $B1 - B10$ of length $l_b = 1.62\,mm - 0.57\,mm$ have been created using *CoventorWare* and the extracted biaxial residual tensile stress from the measurement has been included in the modal analysis. The first three modes have been simulated and compared with the measurements in order to verify the values of the extracted tensile stress. In the simulation, $\rho = 16\,300\,kgm^{-3}$ and $E = 175\,GPa$ have been assumed [56]. In Figure 4.6, the simulated and measured results for the first, second and third modal frequencies of the straight tantalum bridges have been plotted. The simulated resonant frequencies using the extracted residual tensile stress agree well with the measurement results, confirming that the average tensile stress values of $\sim 3\,MPa$ to $\sim 10\,MPa$ exist within the tantalum bridges with length decreases from $1.62\,mm$ to $0.57\,mm$.

4.3.2 Modal shape simulation

The dominant type of motion for each mode i.e. the mode shapes of the straight tantalum bridges in the presence of the extracted residual tensile stress have been investigated using the finite element model simulation. Figure 4.7 illustrates the simulated shapes for the first, second and third mode, $n = 1 - 3$ of the tensile stressed-straight tantalum bridges. All $B1 - B10$ bridges have been simulated and shown to possess the 1st symmetrical bending, 1st antisymmetrical bending and 2nd symmetrical bending motions as the first, second and third mode shape. The

simulation results also correlate well with the resonant frequency measurements, in which the highest displacement amplitude has been measured from the first mode followed by the third and finally the second mode.

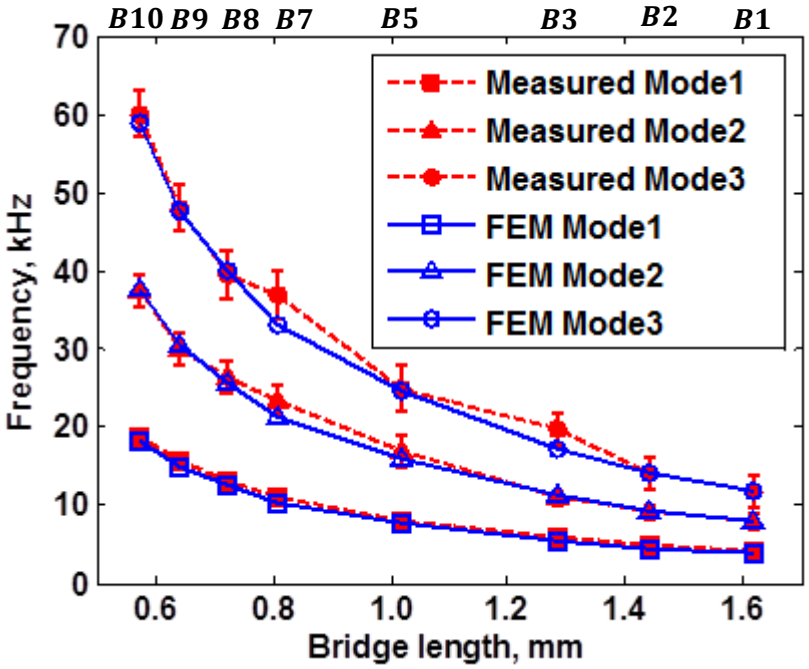
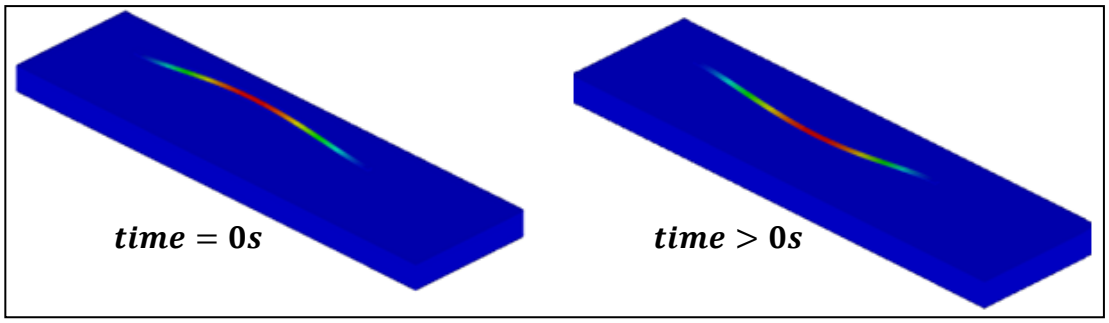


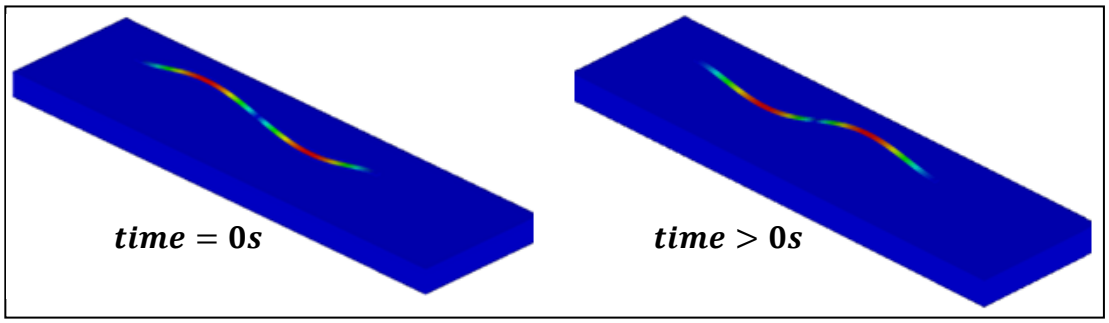
Figure 4.6 *The finite element model (FEM) for modes* $n = 1 - 3$ *have been simulated with respect to the bridge length* $l_b = 1.62\ mm - 0.57\ mm\ (B1 - B10)$ *and agree well with the measurements.*

When the laser beam spot is positioned around the middle region of the bridge length, the antinodes might have been measured for the first and third mode while nodes might have been detected for the second mode. It is essential to determine the antinode positions along the bridge in order to optimise the positioning of channel region underneath the bridge. The channel of RGT can be positioned underneath the antinode of the first vibration mode in order to 1) maximise the mechanical vibration transduction to the channel and 2) to filter out mechanically the unwanted harmonics. At this position, the unwanted second mode might not be detected as much. Around the node position of the second mode, the magnitude is theoretically very small compared to the fundamental vibration. From the frequency measurement, very faint peaks of second mode have been observed around the middle position of the

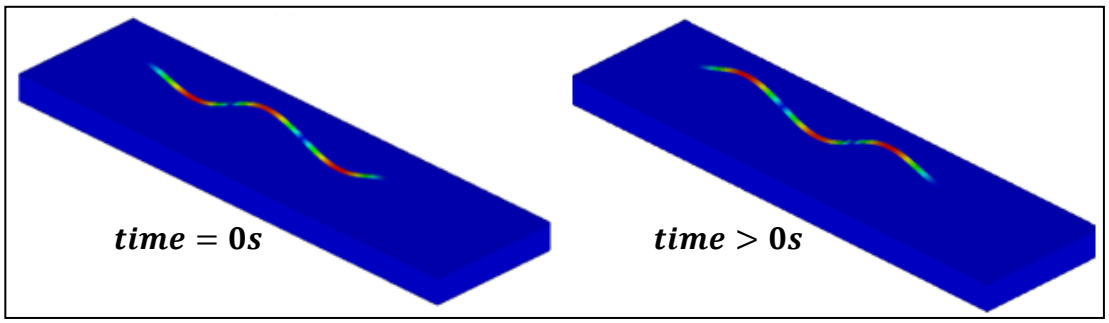
tantalum bridges. The increase of amplitude for the second mode has been noticed as the laser beam spot moved towards the anchor region i.e. towards the antinode of the second mode. The problem with the third mode detection is more significant than the second mode as the antinode also occurred at the same position with the first mode and the magnitude is comparatively high. These unwanted modes can be filtered out electrically.



(a) $n = 1$



(b) $n = 2$



(c) $n = 3$

Figure 4.7 *The (a) first (b) second and (c) third modal shapes of the tensile-stressed tantalum bridge structures have been simulated to possess the 1st symmetrical bending, 1st antisymmetrical bending and 2nd symmetrical bending motions, respectively.*

4.3.3 Mechanical response of tantalum bridges

The mechanical frequency responses of the straight tantalum bridges $B1 - B10$ have been measured in moderate vacuum and air environments. The frequency, displacement and quality factor of the measured first mode in vacuum and air have been studied and compared.

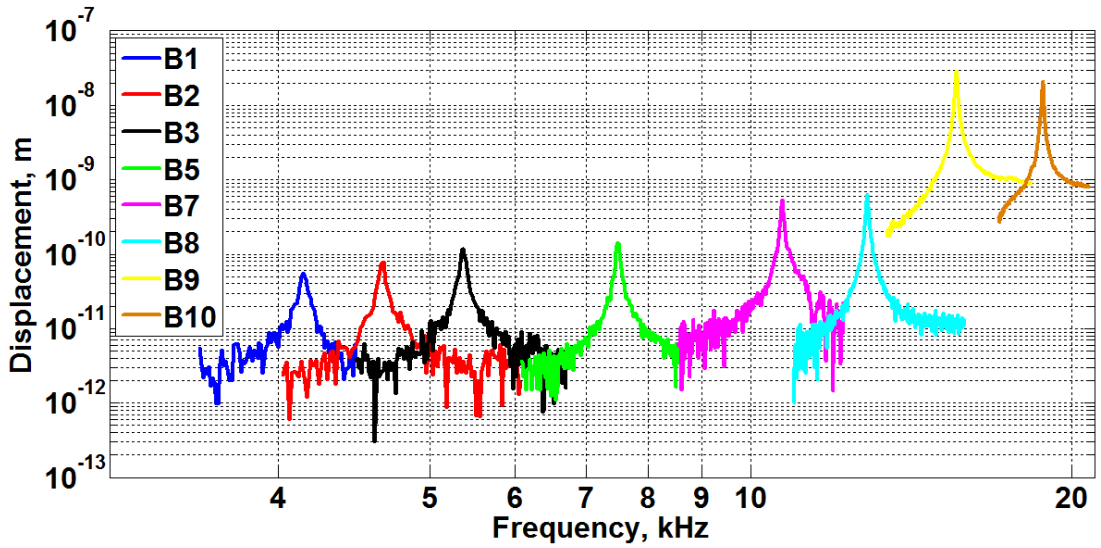
4.3.3.1 In vacuum

The straight tantalum bridges $B1 - B10$ of $w_b = 25\,\mu m$, $t_b = 0.5\,\mu m$ and $l_b = 1.62\,mm - 0.57\,mm$ have been actuated mechanically by applying the AC voltage of $5\,V$ across the piezoelectric disc. The measured mechanical frequency responses of the vibrating bridges in vacuum of pressure $\sim 10\,mTorr$ are plotted in Figure 4.8(a). For the decrease in bridge length from $l_b = 1.62\,mm\,(B1)$ to $l_b = 0.57\,mm\,(B10)$, the first modes of $f_1 = 4.2\,kHz - 18.8\,kHz$ with $0.06\,nm - 100\,nm$ of vibration displacements have been measured. The increase in vibration displacements with the decrease in bridge length is probably related to the increase in the mechanical force per unit area applied onto the bridges.

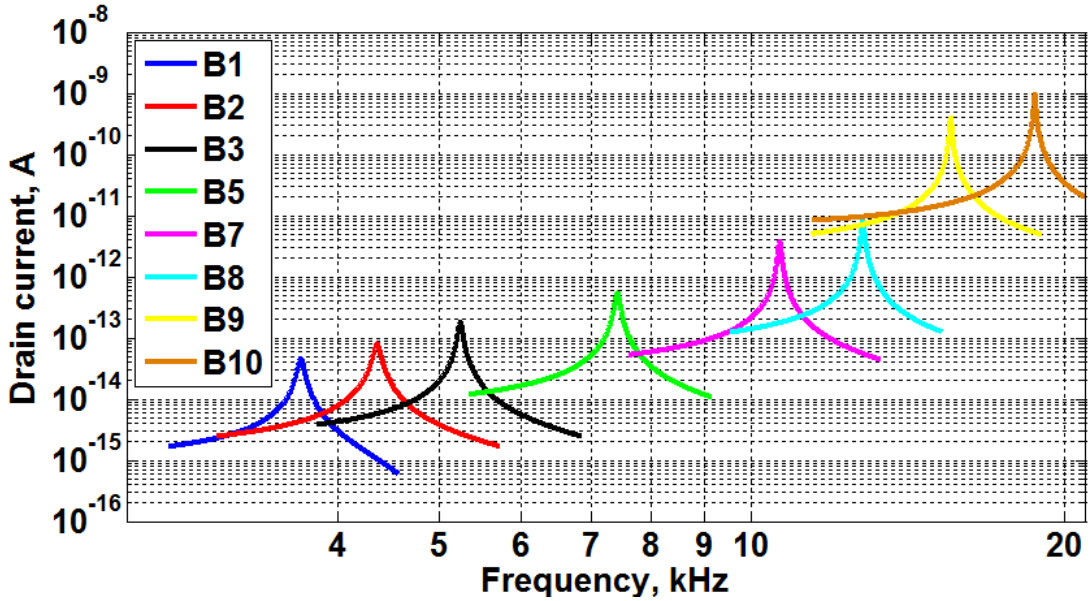
The quality factor of the vibrating bridges has been measured to increase from $Q_{10}\sim 15$ to 85 with respect to decreasing bridge length. The total damping at a constant bridge width has been discussed in sections 2.4.2.1 and 2.6.3 to increase(decrease) as the bridge length increases(decreases), giving smaller(higher) Q_{10}. The mathematical model of RGT described in Chapter 2 and the measured mechanical frequency responses from the straight tantalum bridges $B1 - B10$ in Figure 4.8(a) have been used to calculate the electrical output responses of RGTs.

The mass, damping and stiffness of the straight tantalum bridges have been estimated from the measured frequency responses and then the corresponding equivalent lumped element models have been calculated. The drain current model for RGT working in the saturation regime described in equation 2.19 has been used, assuming $W_c = 5\,\mu m$, $L_c = 25\,\mu m$, $t_{ox} = 70\,nm$ and $\mu = 1400\,cm^2/Vs$ [refer section 2.4.4]. In the model, the distance of the bridge gate to channel region is fixed at $\sim 3.4\,\mu m$.

The applied voltage onto the bridge gate has been assumed to be $V_{gs} = \frac{2}{10} V_{pi}$ with the threshold voltage of $V_{th} = \frac{1}{10} V_{pi}$, in order to satisfy $V_{th} < V_{gs} < V_{pi}$.



(a) Measured mechanical responses of $B1 - B10$ in vacuum



(b) Calculated electrical responses of $B1 - B10$

Figure 4.8 *(a) The measured frequency responses of the straight tantalum bridges $B1 - B10$ in vacuum. The quality factor has been measured to increase from Q_{10}~15 to 85 with respect to the decrease in bridge length from $l_b = 1.62\ mm$ ($B1$) to 0.57 mm ($B10$). (b) Using the mathematical model of RGT, the drain current responses have been calculated from the measured mechanical frequency responses in (a).*

The expected drain current responses in frequency domain from the RGTs with straight tantalum bridges $B1 - B10$ are calculated and plotted in Figure 4.8(b). The drain current has been calculated to increase from $48\ fA$ to $1\ nA$ as the bridge length decreases from $l_b = 1.62\ mm$ $(B1)$ to $l_b = 0.57\ mm$ $(B10)$. The calculated drain currents are considerably small, thus higher V_{gs} and/or larger bridge vibration displacement are desired in order to draw out measurable current amplitudes from the RGTs.

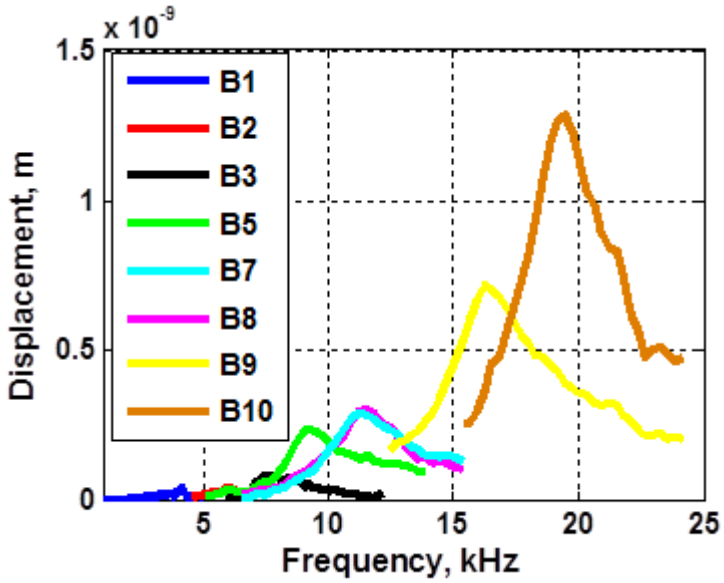
4.3.3.2 In air

The frequency measurement of the straight tantalum bridges $B1 - B10$ have been carried out in the standard atmospheric pressure of $\sim 760\ mTorr$. In Figure 4.9(a), similar range of first modes $f_1 = 4.2\ kHz - 18.8\ kHz$ with those measured in vacuum has been detected while the ranges for vibration displacement $(0.04\ nm - 1.3\ nm)$ and quality factor $(Q_{10} \sim 1 - 3)$ have been measured to be smaller. The comparison between the measured resonant peak in air and vacuum for $B10$ of length $l_b = 0.57\ mm$ is shown in Figure 4.9(b).

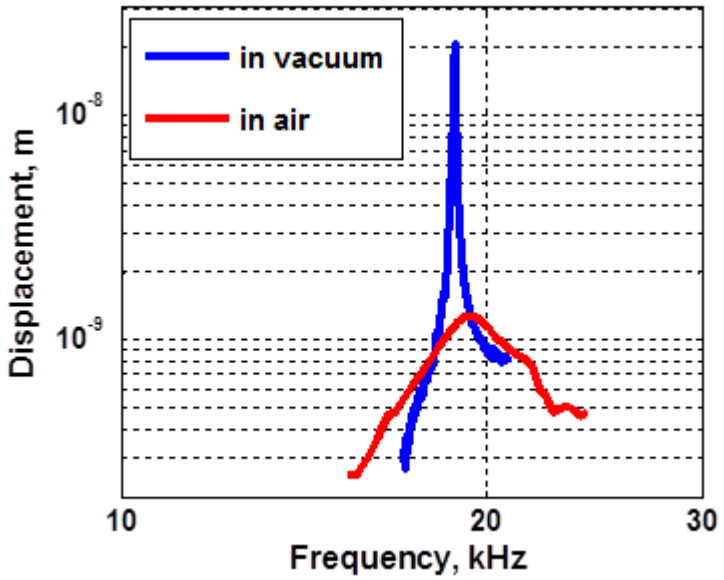
In Figure 4.9(b), the quality factor of the tantalum bridge decreases from $Q_{10} \sim 85$ in vacuum to $Q_{10} \sim 3$ in air. The large difference in the measured quality factor is due to the influences of the viscous forces from the surrounding air that dampen the bridge movement and thus reduce the quality factor [16][27][28]. The effect of air damping has also reduced the mechanical vibration displacement of the bridge from $100\ nm$ to $1.3\ nm$.

For the RGT cochlear biomodel application, the measured frequency responses from the fabricated straight tantalum bridges operating in air are fairly acceptable and quite similar with the frequency responses of the basilar membrane measured by others with the quality factor of $Q_{10} \sim 0.6 - 10$ and the vibration displacements in $2\ nm - 20\ nm$ range [5][6]. In future, higher quality factor and vibration displacement from the fabricated tantalum bridge structure could be achieved by

manipulating the bridge width as discussed in section 2.6.3.1 and/or adjusting the air pressure to be slightly smaller than $\sim 760\ mTorr$.



(a) Measured mechanical responses of $B1 - B10$ in air



(b) Measured mechanical response of $B10$ in air and vacuum

Figure 4.9 *(a) The measured mechanical frequency responses of the straight tantalum bridges $B1 - B10$ in open air. The quality factor has been measured to increase from $Q_{10}\sim 1$ to 3 with respect to the decrease in bridge length from $l_b = 1.62\ mm$ $(B1)$ to $0.57\ mm$ $(B10)$. (b) Comparison between the measured resonant peak of $B10$ in vacuum and air.*

4.4 Characterisation of buckled tantalum bridges

Imperfections in fabrication have been reported to induce residual stress within the sputter-deposited thin film layer [71]-[75]. The presence of stress within the sputter-deposited layer has been seen to influence the mechanical behaviour, as have been measured previously from the straight tantalum bridges in which the tensile stress has caused the resonant frequencies to be many times higher than the theoretical values. The presence of residual stress can also be detected visually from the physical deformation of the released structures. The influence of biaxial residual compressive stress and bridge length on bridge deflection have been simulated and discussed in section 3.6.3 for the aluminium bridges. The biaxial residual compressive stress has been discovered to cause the bridge to deflect upwards [71]-[75]. At a constant value of compressive stress, the vertical upwards bridge deflection increases with the increase in bridge length [71][74].

The flaws in the material's growth process and thermal effect on the material layer are some of the fabrication imperfections that can build up the residual compressive stress within the bridge structure [74][75][78]. The anchors are constrained from moving axially and thus, the built up compressive stress would reach a critical value in which out-of-plane deformation occurred on the bridge [75]. The buckled bridges have been studied in order to determine the exhibited residual compressive stress within the structural material [71]-[75].

For our fabricated buckled tantalum bridges, the residual compressive stress within the sputter-deposited tantalum layer has been investigated using two techniques. The wafer curvature technique has been carried out in order to determine the total compressive stress of the sputter-deposited tantalum layer on a 3-inch wafer. Then, the compressive stress within the sputter-deposited tantalum bridge structure has been determined by measuring the maximum vertical deflection of the buckled structures. Static model analysis of the buckled tantalum bridge structure has been conducted. Finally, the measured frequencies from the buckled tantalum bridges

have been compared with the FEM modal analysis and the corresponding modal shapes have been simulated.

4.4.1 Residual stress-induced tantalum layer

In wafer curvature technique, the wafer bending before and after the deposition of tantalum layer is measured. After measuring the curvature, Stoney's equation [equation 4.2] has been used to estimate the total residual stress σ in the tantalum film layer which has been sputtered on a $< 100 >$ silicon wafer [77]; where E_{si}, ν_{si} and t_{si} being the Young's modulus, Poisson's ratio and thickness of the silicon substrate wafer, R_b and R_a being the silicon wafer's curvature radius before and after the tantalum sputter-deposition process and t_b is the sputter-deposited tantalum layer thickness [60][62][78].

The measurement of wafer curvature has been carried out using DEKTAK 8000 surface profilometer. The curvature along the x-axis (left to right) and y-axis (top to bottom) of the wafer with respect to the flat cut for $< 100 >$ have been measured and averaged. The measured residual stress represents the total average stress of tantalum layer across the 3-inch wafer. Negative value of σ corresponds to compressive stress that induces convex curvature on the wafer while positive σ represents tensile stress that causes the concave curvature on the wafer [62].

$$\sigma = \frac{E_{si}{t_{si}}^2}{6(1-\nu_{si})t_b}\left(\frac{1}{R_a}-\frac{1}{R_b}\right) \tag{4.2}$$

Sputter-deposition is a technique of ejecting the material atoms from a target source and depositing them as a thin film material layer on a substrate at certain conditions of pressure and temperature [79][80]. In our tantalum sputter-deposition process, $50\ sccm$ of argon gas is fed into the DC magnetron sputtering tool and electric field is applied to create the argon plasma. The generated argon ions are bombarded towards the 99.9% pure tantalum target. The tantalum atoms are then removed physically from the target and transported onto the silicon wafer where the tantalum atoms will condense, forming a thin film layer. The crystallographic microstructures

and the induced residual stress in the tantalum layer grown by the sputter-deposition process depend strongly on various process conditions such as the species used as the sputtering gas (argon, xenon, etc), the energy of the bombarded ion particles, the substrate temperature and the voltage applied onto the substrate [55][56][59][61][62][68].

4.4.1.1 Influence of argon gas pressure and tantalum thickness on residual stress

In this study, the effect of varying the working pressure of the sputtering argon gas is investigated. The argon gas sputtering pressure has been reported to be able to control the energy of the sputtered tantalum atoms and/or the rebound/reflected neutralised argon ions from the target towards the substrate. The neutralised argon ions might also be trapped within the growing tantalum layer. Low(high) argon gas sputtering pressure promotes high(low) energy of tantalum atoms and/or neutralised argon ion bombardments [78].

The tantalum layers with thickness of $0.3\,\mu m$ and $0.5\,\mu m$ have been sputter-deposited onto the silicon wafer substrate under the argon gas pressure of $3\,mTorr$ and $15\,mTorr$. The measured residual stresses are tabulated in Table 4.1. The result shows that for $0.5\,\mu m$ of tantalum thickness, the measured residual stress has been found to be compressive under both argon gas pressure conditions. The compressive stress of tantalum at $15\,mTorr$ is lower than the compressive stress measured at $3\,mTorr$. Thus, the decreasing of argon gas pressure has been seen to build up the compressive stress within the tantalum layer. Similar trend of stress has been observed for the tantalum layer of $0.3\,\mu m$ thickness. The residual stress at $15\,mTorr$ has been measured to be tensile. In similar manner, the effect of decreasing the argon gas pressure from $15\,mTorr$ to $3\,mTorr$ has built up the compressive stress within the layer, changing the stress from tensile to compressive.

In addition, the effect of increasing the tantalum layer thickness at a constant argon gas pressure has been observed to have similar results with the effect of decreasing the argon gas pressure at constant tantalum layer thickness. At $15\,mTorr$, the

transition of stress from tensile to compressive has been measured as the thickness increases from $0.3\,\mu m$ to $0.5\,\mu m$ while at $3\,mTorr$, the induced residual compressive stress increases.

Wafer no.	Argon pressure ($mTorr$)	Thickness (μm)	Stress (MPa)
1	3	0.5	-327
2	3	0.5	-302
3	15	0.5	-131
4	15	0.5	-219
5	3	0.3	-175
6	15	0.3	135
7	15	0.3	18

Table 4.1 *The measurement of the total average stress for* $0.3\,\mu m - 0.5\,\mu m$ *of tantalum film layers with* $3\,mTorr - 15\,mTorr$ *of argon gas sputtering pressures.*

Most sputter-deposited thin film metals have been reported to possess the general trend of transition from an intrinsic tensile stress to compressive stress as the working pressure decreases [82][68][65][63][59]. Thornton *et al* have published that the sputter-deposited tantalum layers of $0.2\,\mu m$ thickness at low argon gas pressure ($\sim 3\,mTorr$) are in compressive stress ($\sim -1.5\,GPa$) while at high pressure ($\sim 20\,mTorr$), the tantalum layers are in tensile ($\sim 750\,MPa$) [82]. The trend is comparable with our measured results for $0.3\,\mu m$ of tantalum thickness. Additionally, Clevenger *et al* have reported on the increase in intrinsic compressive stress for tantalum from $-500\,MPa$ to $-2\,GPa$ with the decrease in sputtering argon gas pressure from $90\,mTorr$ to $3\,mTorr$ [59]. Similar observation has been seen from our measurement results for $0.5\,\mu m$ of tantalum thickness in Table 4.1. Finally, the influence of material layer thickness on the induced stress has also been reported in [82], where the increase in compressive stresses have been observed when the tantalum layer thickness increases from $0.05\,\mu m$ to $0.3\,\mu m$, under all

argon gas pressure conditions from $1\,mTorr$ to $15\,mTorr$. Similar increase in compressive stress has been observed from our measurement results for the sputter-deposited tantalum layer at $3\,mTorr$ with the thickness increases from $0.3\,\mu m$ to $0.5\,\mu m$.

The build up of compressive stress within the sputter-deposited tantalum layer has been explained using the atomic-peening model [60][82][78] in which the argon and/or tantalum atoms bombardments had compressed the growing tantalum layer. At low argon gas pressure, the highly energetic tantalum atoms can penetrate the growing tantalum layer to remain under the metal surface, and thus densifying the layer [81]. In addition, the bombardments of the highly energetic argon atoms have assisted the densification process during the tantalum film growth, leading to the generation of compressive stress within the layer. The metal layer under compressive stress has been reported to possess the densely-packed microstructures with no porosity [59][60][63][64][82].

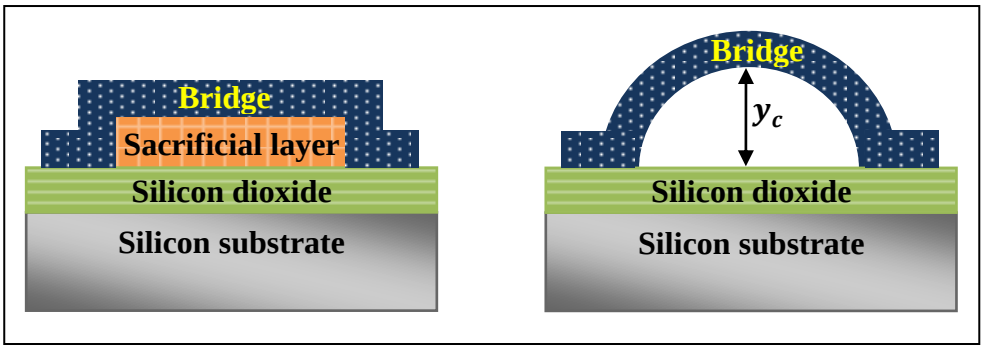
On the contrary, at high argon gas pressure, the effect of argon atoms bombardment decreases and the low energy tantalum atoms have been postulated to remain at the metal surface during the growth of tantalum layer, producing a porous microstructure layer with tensile stress. The grain boundary attraction mechanism has been proposed to explain the tensile stress generation. As the layer grows, the grain coalesces and eliminates the grain boundaries, decreasing the volume of the metal layer and thus generating the tensile stress [63][78]. Therefore, argon gas pressure has been seen to be able to control the energy of atom bombardments on the growing metal surface layer which affects the microstructure of the evolving layer and thus the stress generation [60][82][78][81].

For the bridge fabrication, the sputter-deposition process of the tantalum layer has been set at $3\,mTorr$ with $0.5\,\mu m$ of bridge thickness. From the wafer curvature measurement, the estimated total stress of the tantalum layer on a 3-inch silicon wafer is $\sim -310\,MPa$. Thus, the fabricated tantalum bridge structure is expected to be under the influence of the biaxial residual compressive stress. However, the

subsequent processing steps to fabricate the bridge structure from the sputter-deposited tantalum layer might either increase the induced compressive stress or transform it into tensile. Next, the static analysis of the fabricated buckled tantalum bridges has been carried out and the magnitude of the biaxial residual compressive stress within the structure has been extracted.

4.4.2 Compressive stress-induced bridges

The physical deformation of microstructures can be used to determine the residual stress within the structural material layer [71]. The *in situ* residual stress measurement technique using the small microstructures like cantilevers and bridges are able to measure and map the local stress, unlike the wafer curvature measurement technique that only measures the total average residual stress of the material layer on the whole wafer [72]. In this study, the static deformation measurement of the fabricated buckled tantalum bridges will be carried out in order to determine a more accurate value of the induced residual compressive stress within the tantalum layer of the bridge structure at the dimensional scale of interest.



(a) Compressed state **(b)** Post-buckled state

Figure 4.10 *The conditions of the originally flat bridge structure that is being subjected to the biaxial residual compressive stress beyond the critical buckling value (a) before and (b) after the released stage.*

In Figure 4.10(a), the patterned bridge structure on a sacrificial layer before being released is under the compressed state if the biaxial residual compressive stress exists within the structure. In Figure 4.10(b), the released bridge with two fixed ends

will buckle and stay in the post-buckled configuration if the induced compressive stress within the structure went beyond a critical value [69][73]. Before the buckling point, the compressively stressed bridge will be released without vertical deflection as have been seen previously from the fabricated aluminium bridge structures of length $0.092\,mm$ and $0.278\,mm$ in section 3.6.2. The critical buckling value depends on the bridge's geometry. Kobrinsky *et al* have introduced the critical biaxial residual compressive stress value as a function of bridge length [71]. Other than the residual stress, the imperfections of boundary condition might also have contributed to the bridge deformation [71].

4.4.2.1 Static analytical model for bridge vertical deflection

Kim *et al* and Bouwstra *et al* have presented the static model for the buckled bridge structure with fixed-fixed ends [66][76]. In the model, the induced compressive axial force beyond the buckling point at the anchor ends causes the uniaxial elastic elongation of the bridge. As the bridge length increases, the excess length is relaxed by the increase of the bridge's central vertical deflection rather than the increase in the induced stress [66][76]. The central vertical deflection of the fabricated buckled tantalum bridges in Figure 4.2 has been observed to increase with the increase in bridge length.

The analytical solution for the central vertical deflection, y_c of an originally flat, fixed-fixed bridge subjected to the biaxial residual compressive stress σ_{comp} beyond the critical buckling load is given by equation 4.3 with l_b, t_b, υ, E represents the length, thickness, Poisson's ratio and Young's modulus of the bridge [66][69][76]. y_c of the fabricated buckled tantalum bridge structures have been measured using both the scanning electron microscopy (SEM) and the interferometric profilometry.

$$y_c = \pm\frac{t_b}{\frac{1}{2}\sqrt{3}}\sqrt{\frac{-\sigma_{comp}/E\,/(1-\upsilon)}{\frac{\pi^2}{3}\frac{1}{1-\nu^2}\left(\frac{t_b}{l_b}\right)^2}-1}\sqrt{\left(\frac{1}{1-\nu^2}\right)} \qquad (4.3)$$

An example of the measured bridge profile from the interferometer for $B10$ of length $l_b = 0.57\ mm$ and width $w_b = 30\ \mu m$ is shown in Figure 4.11. The central vertical deflection for $B10$ has been measured to be $y_c = 19.9\ \mu m$. The post-buckled shape of the bridge is in the form of the first symmetrical bending mode.

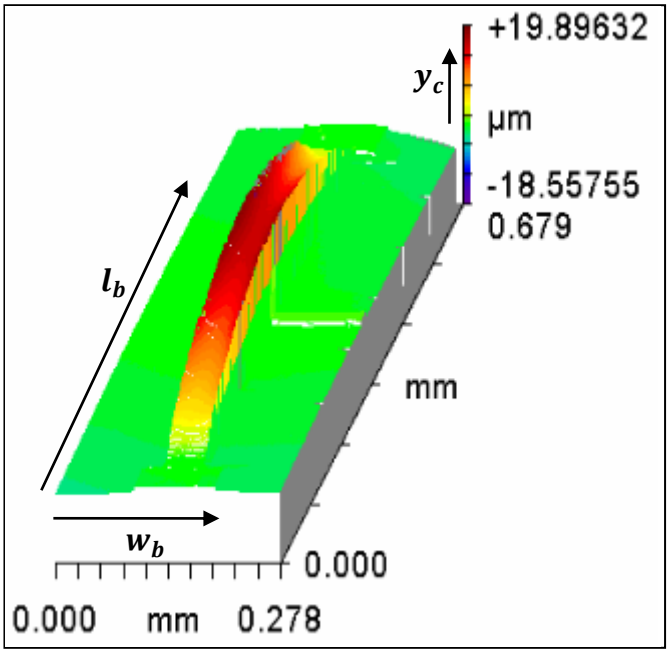


Figure 4.11 *Using interferometric profilometry, the measured y_c for $B10$ of $l_b = 0.57\ mm$ and $w_b = 30\ \mu m$ is $\sim 19.9\ \mu m$. The post-buckled shape of the bridge is in the form of the first symmetrical bending mode.*

For the buckled tantalum bridges $B1 - B10$, the measured y_c decreases from $\sim 60\ \mu m$ to $\sim 20\ \mu m$ with the decrease in bridge length from $l_b = 1.62\ mm$ to $l_b = 0.57\ mm$. The biaxial residual compressive stress σ_{comp} within the buckled tantalum bridges has been extracted from equation 4.3 using the measured central vertical deflection y_c of the bridge in its post-buckled state.

In Figure 4.12, the best fit between the analytical models of y_c at $\sigma_{comp} = -750\ MPa$ to $-950\ MPa$ and the measured y_c is when $\sigma_{comp} = -850\ MPa$. Thus, the extracted biaxial residual compressive stress for the buckled tantalum bridges $B1 - B10$ has been estimated to be $\sigma_{comp} = -850\ MPa$.

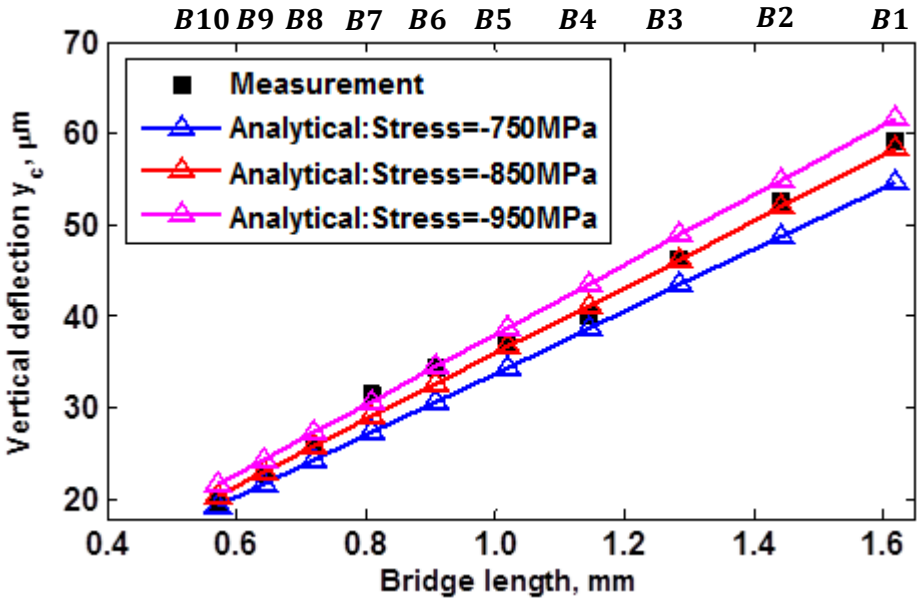


Figure 4.12 *The best fit between the measurement and analytical models of y_c for tantalum bridges $B1 - B10$ is at $\sigma_{comp} = -850\ MPa$.*

4.4.2.2 FEM simulation for bridge vertical deflection

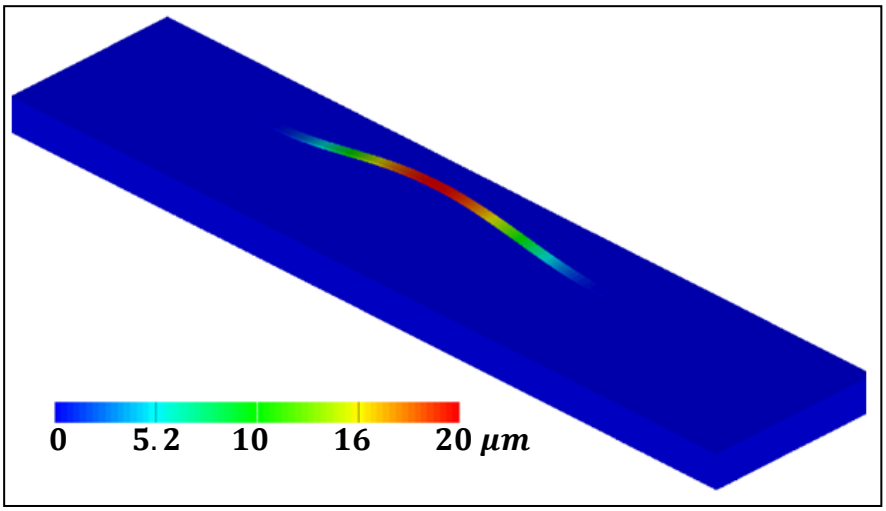


Figure 4.13 *The constructed finite element model for $B10$ under the influence of the biaxial residual compressive stress beyond the critical buckling point of $\sigma_{comp} = -850\ MPa$, giving $y_c = 20.34\ \mu m$.*

The finite element model of the tantalum bridge with buckled geometry has been created for $B10$ as shown in Figure 4.13 with $\sigma_{comp} = -850\ MPa$. The vertical

deflection y_c of the bridge due to the presence of the biaxial residual compressive stress beyond the critical buckling load has been simulated to be $20.34\ \mu m$. The finite element models have also been created for the buckled tantalum bridges $B1 - B9$ in order to simulate y_c. The finite element model simulation results have been compared with the analytical model. The two models agree fairly well with small percentage difference of less than 2.5 %.

4.4.3 Frequency measurement and characterisation of the modal shapes

The buckled tantalum bridges $B1 - B10$ of length $l_b = 1.62\ mm - 0.57\ mm$ have been actuated mechanically and the detected three lowest frequencies have been measured from the bridges. The laser beam spot has been placed at the central vertical deflection of the bridge during frequency measurement.

Then, modal analyses have been performed using the finite element models of the buckled tantalum bridges under the influence of the biaxial residual compressive stress beyond the critical buckling load of $\sigma_{comp} = -850\ MPa$ [69]. The comparison between the simulated modes of $n = 1 - 6$ and the measured three lowest frequencies from the buckled tantalum bridges $B1 - B10$ is plotted in Figure 4.14.

The lowest measured frequencies from the buckled tantalum bridge structures fit the simulated second modes $(n = 2)$ from the finite element models. Furthermore, the second and third lowest measured frequencies fit the simulated fourth $(n = 4)$ and sixth $(n = 6)$ modes, respectively. This indicates that the detected three lowest frequencies measured at the central vertical deflection of the buckled tantalum bridges $B1 - B10$ might correspond to the second, fourth and sixth vibration modes of the bridge.

For the simplification of our analysis, the buckled bridge structure has been assumed to possess perfectly rigid end supports and the contribution from the compliances of the anchor supports have not been included in the analysis.

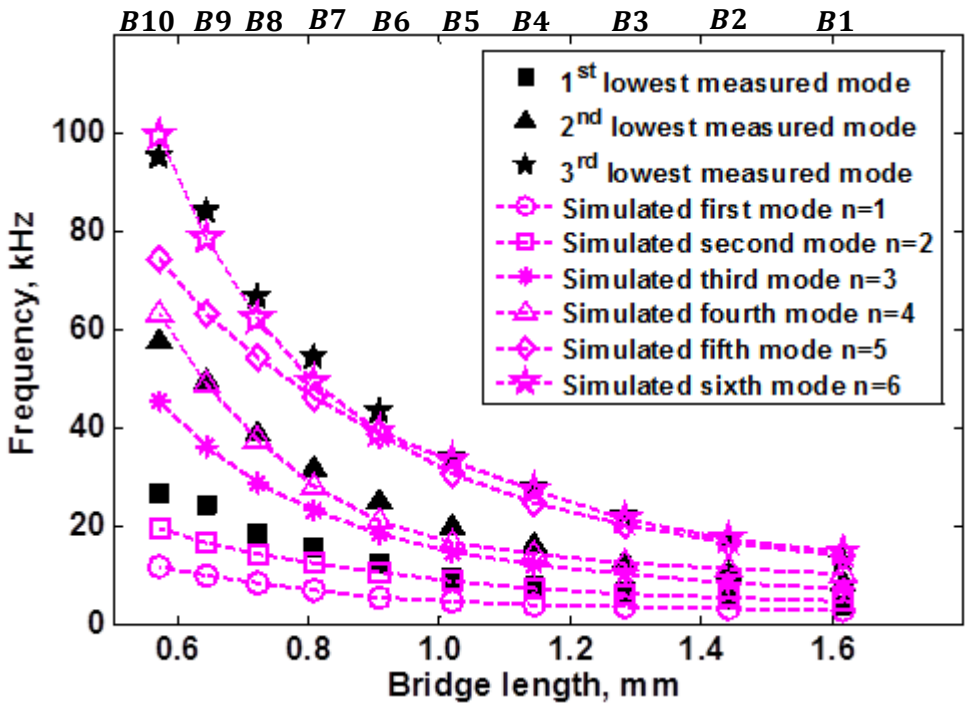


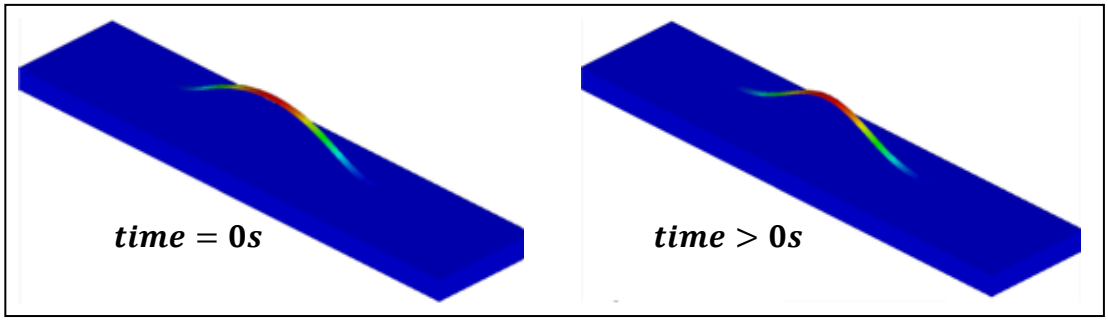
Figure 4.14 *The measured three lowest frequencies from the buckled tantalum bridges $B1-B10$ fit the simulated second, fourth and sixth modes of the finite element models.*

4.4.3.1 Influence of bridge curvature on modal shapes

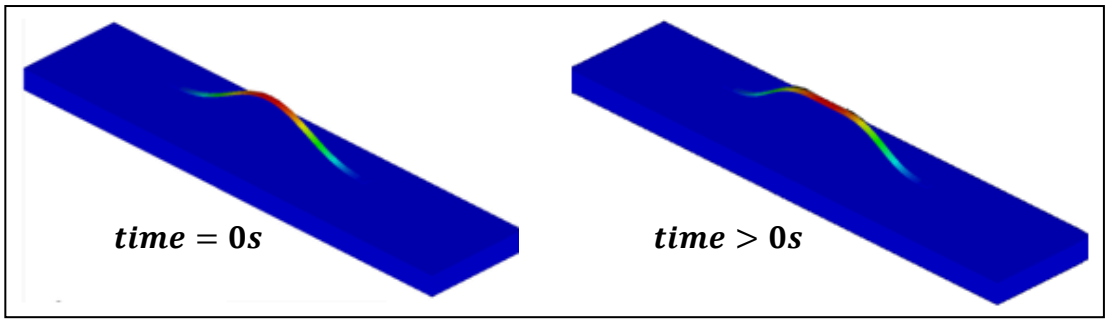
From finite element model of the buckled tantalum bridge structures, the modal shapes i.e. dominant types of motion for modes $n = 1-6$ have been simulated to be the 1st antisymmetrical bending, 2nd symmetrical bending, 2nd antisymmetrical bending, 3rd symmetrical bending, 1st torsional bending and 3rd antisymmetrical bending motion, respectively. The buckled structures possess the stretch–bending elastic coupling that is proportional to the curvature [84]. Due to the bridge curvature, the mode transition phenomenon occurred in which the mode sequence and the corresponding dominant type of motion exchanged. This explains the disappearance of the 1st symmetrical bending motion as the first mode [84].

The simulated modal shapes for the second, fourth and sixth modes of vibration of the buckled tantalum bridges in the presence of $\sigma_{comp} = -850\ MPa$ are shown in Figure 4.15. For these vibration modes, the buckled structures are seen to vibrate transversely, in-plane with the bridge curvature. The transverse motions of vibration

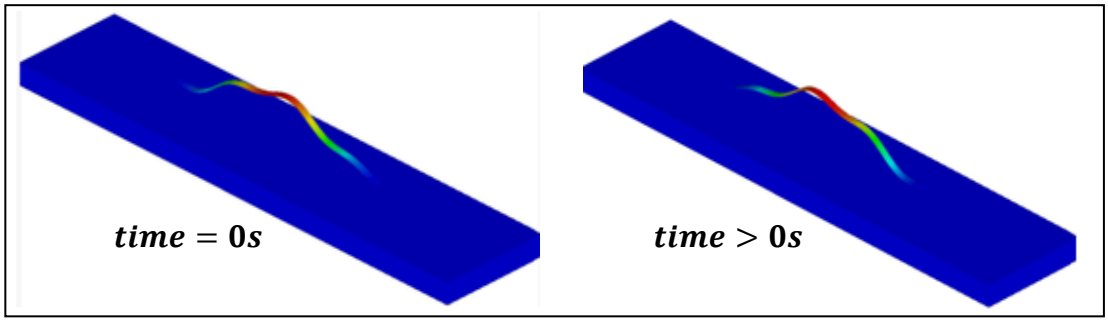
are detectable and measurable by the laser. On the other hand, the first, third and fifth vibration modes of the buckled structures might not have been detected by the laser which has been positioned at the central vertical deflection of the bridge. Figure 4.16 shows the corresponding simulated modal shapes for the first, third and fifth modes of bridge vibration.



(a) $n = 2$

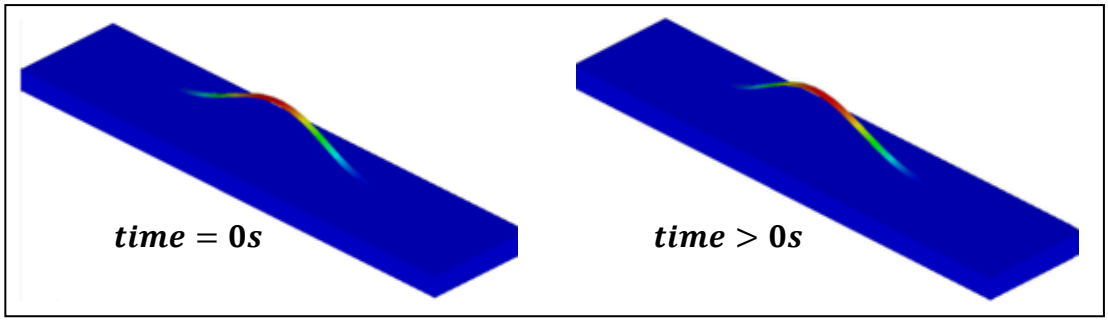


(b) $n = 4$

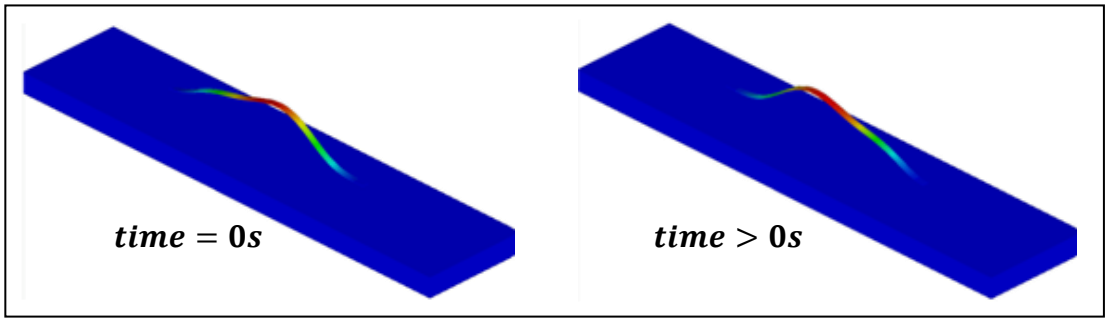


(c) $n = 6$

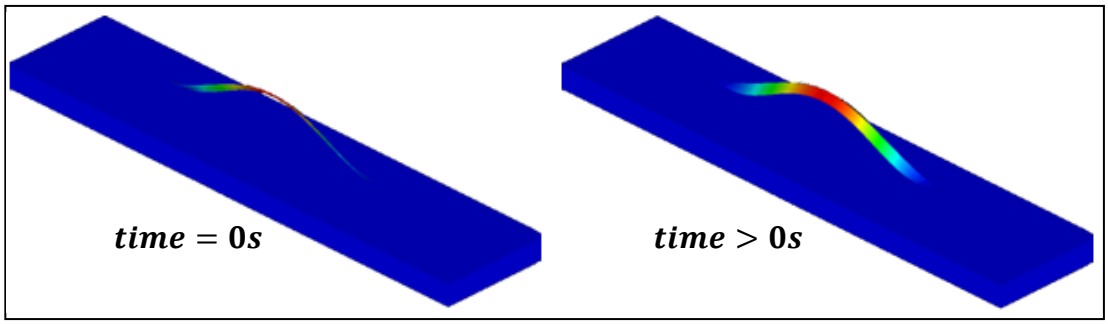
Figure 4.15 *The (a) second (b) fourth and (c) sixth modal shapes of the compressive-stressed buckled tantalum bridge structures have been simulated to possess the 2nd symmetrical bending, 3rd symmetrical bending and 3rd antisymmetrical bending motion, respectively. The bridges vibrate transversely.*



(a) $n = 1$



(b) $n = 3$



(c) $n = 5$

Figure 4.16 *The (a) first (b) third and (c) fifth modal shapes of the compressive-stressed buckled tantalum bridge structures have been simulated to possess the 1st antisymmetrical bending, 2nd antisymmetrical bending and 1st torsional bending motion, respectively. The bridges vibrate longitudinally.*

For the first, third and fifth modes of bridge vibration, the buckled structures are seen to vibrate longitudinally, out-of-plane from the bridge curvature. Therefore, this explains the fitting of the measured three lowest frequencies at the central vertical deflection of the buckled tantalum bridges with the simulated second, fourth and

sixth modes as the first, third and fifth modes of the bridge vibration might not have been detected by the laser.

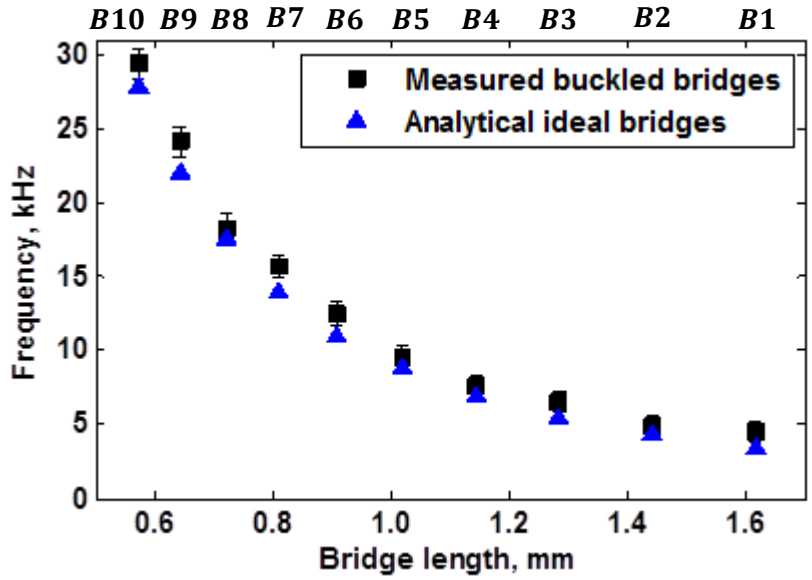
In order to obtain maximal vibration transduction from the tantalum bridge to the channel region of RGT, the positioning of the channel underneath the buckled tantalum bridge gate would be at the antinodes of the second mode. Since the distance of the bridge gate to the channel depends on the buckling behaviour of the tantalum bridge, the threshold voltage for the channel will be affected significantly.

4.4.3.2 Influence of bridge curvature on frequency

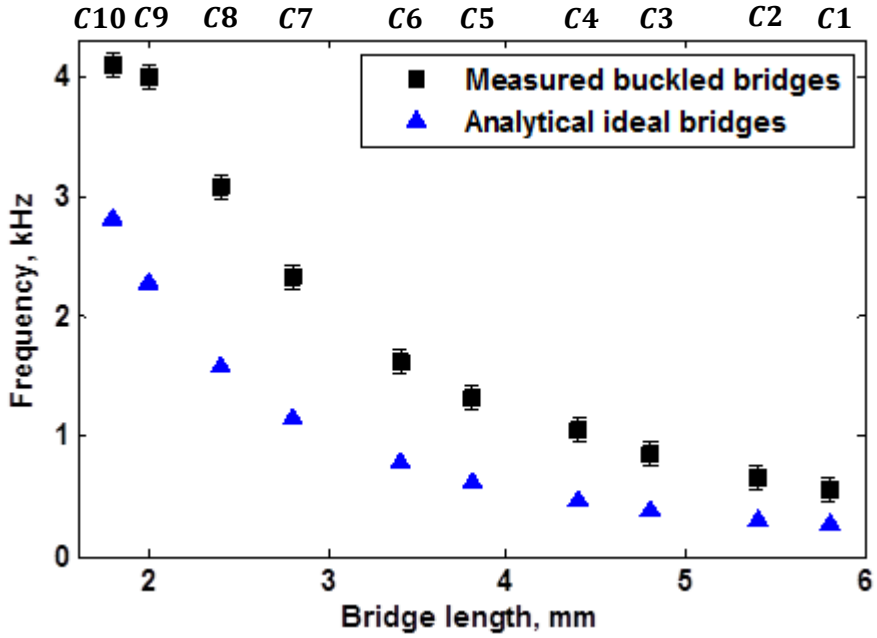
The second mode for the buckled tantalum bridges $B1 - B10$ of length $l_b = 1.62\,mm - 0.57\,mm$ from Figure 4.14 have been measured to be $4.5\,kHz$ to $29.4\,kHz$. The buckled tantalum bridges $C1 - C10$ of length $l_b = 5.8\,mm - 1.8\,mm$ have also been actuated mechanically and the measured second mode of $550\,Hz$ to $4.1\,kHz$ have been plotted in Figure 4.17(b).

The corresponding modal shape for the second mode has been simulated to possess the 2nd symmetrical bending motion. In addition, the analytical mode for the unbuckled stress-free tantalum bridges with 2nd symmetrical bending motion have also been calculated and compared with the measurements in Figure 4.17. For all compressive-stressed buckled tantalum bridge structures, the measured modes are $\sim 1.1 - 2$ times higher compared to the ideal, straight and stress-free tantalum bridges.

The study in flexural vibration for the straight bridges or bridges with small curvatures $\left(\frac{y_c}{t_b} < 1.2\right)$ has shown that the presence of compressive stress within the structures have caused the symmetrical and antisymmetrical modes of the bridges to be smaller than the unbuckled stress-free bridges [66][76]. However, the increase in bridge curvature can affect the resonant frequencies of the bridge. Kim *et al* have reported that all symmetrical modes tend to increase as the curvature effect increases. This is due to the bridge vibrations which are not orthogonal to the shape of the curvature [76].



(a) $B1 - B10$



(b) $C1 - C10$

Figure 4.17 *The second mode with 2^{nd} symmetrical bending motions for the compressive-stressed buckled tantalum bridges of length (a) $l_b = 1.62\ mm - 0.57\ mm$ $(B1 - B10)$ and (b) $l_b = 5.8\ mm - 1.8\ mm$ $(C1 - C10)$ have been measured to be $\sim 1.1 - 2$ times higher than the calculated frequencies of the ideal unbuckled stress-free tantalum bridges with 2^{nd} symmetrical bending motions.*

Therefore, for bridges with large curvature $\left(\frac{y_c}{t_b} > 1.2\right)$, the curvature effect dominates over the compressive stress effect causing the bridges to have higher symmetrical modes compared to the unbuckled stress-free bridges [76]. In our case, the fabricated tantalum bridge structures which exhibit considerably large central vertical deflections are categorised into the curvature effect domination regime. This explains the fact that the measured symmetrical second mode of the compressive-stressed buckled tantalum bridges to be higher than the ideal, straight and stress-free tantalum bridges.

4.5 Conclusion

In this chapter, the tantalum metal has been pursued as the material structure for the bridges due to its superior material properties compared to aluminium. The employment of tantalum has solved the sagging and collapsing issues of the released aluminium bridges in Chapter 3. The tantalum bridges of length $l_b = 0.57\,mm - 5.8\,mm$ have been released successfully from the photoresist sacrificial layer of $3.4\,\mu m$ thickness using the developed downstream oxygen/nitrogen plasma etch release technique. The fabricated tantalum bridges have been released free-standing and possess either the straight or buckle profile. The inconsistent profile behaviour of the fabricated tantalum bridge structure is probably due to the induced biaxial residual stress within the tantalum layer during the tantalum sputter-deposition process and/or other subsequent processing steps. In addition, the induced biaxial residual stresses within the bridges have affected the modal behaviour of the structures.

For the straight tantalum bridges, the first modes have been measured to be four to six times higher than the analytical stress-free tantalum bridges. Thus, the fabricated straight bridges have been suspected to be under the influence of the biaxial residual tensile stress. The values of tensile stress have been extracted by fitting the first, second and third modes of the analytical tensile-stressed tantalum bridges to the measurement. The tensile stress has been found to increase from $\sim 3\,MPa$ to

$\sim 10\ MPa$ with the decrease of the tantalum bridge length from $1.62\ mm$ to $0.57\ mm$. In addition, the simulated first, second and third modes from the finite element models have been found to fit well with the measurements, thus validating the extracted tensile stress values. The tensile-stressed straight tantalum bridges have been simulated to possess the 1st symmetrical bending, 1st antisymmetrical bending and 2nd symmetrical bending motions as the first, second and third modal shapes. In moderate vacuum, the first modes of the straight tantalum bridge structures with $l_b = 1.62\ mm - 0.57\ mm$ have been measured to be $4.2\ kHz - 18.8\ kHz$ with $0.06\ nm - 100\ nm$ of vibration displacement and $Q_{10} \sim 15 - 85$ of quality factor. In standard atmospheric pressure, the first modes have been measured to possess smaller vibration displacement ($0.04\ nm - 1.3\ nm$) and quality factor ($Q_{10} \sim 1 - 3$) due to air damping. The measured quality factor of the straight tantalum bridges operating in air has been found to be suitable for RGT cochlear biomodel application.

For the buckled tantalum bridges, the induced biaxial residual compressive stress within the tantalum layer has been found to be responsible for deflecting the bridges upwards. From the wafer curvature measurement technique, the total average compressive stress within the sputter-deposited tantalum layer has been determined to be $-310\ MPa$. The effects of decreasing the argon gas pressure and increasing the tantalum layer thickness during the sputter-deposition process have been found to 1) transform the residual stress from tensile to compressive and 2) build-up the existing compressive stress within the tantalum layer. The fabricated buckled tantalum bridges of length $l_b = 1.62\ mm - 0.57\ mm$ have been measured to possess the central vertical deflection of $y_c \sim 60\ \mu m - 20\ \mu m$. From y_c, the biaxial residual compressive stress within the tantalum bridges has been extracted to be $-850\ MPa$. The detected and measured frequencies from the compressive-stressed buckled tantalum bridge structures have been simulated to be the second, fourth and sixth bridge vibration modes with the corresponding modal shapes of the 2nd symmetrical bending, 3rd symmetrical bending and 3rd antisymmetrical bending motions, respectively. The symmetrical second mode of the compressive-stressed

buckled tantalum bridges of length $l_b = 5.8\,mm - 0.57\,mm$ have been measured to be $550\,Hz - 29.4\,kHz$. The measured modes are $\sim 1.1 - 2$ times higher than the analytical modes from the ideal, straight and stress-free tantalum bridges due to the bridge curvature effect.

Chapter 5: Design and characterisation of *n*-type channel and source /drain for enhancement and depletion mode *n*-MOSFET

5.1 Introduction

In Chapters 1-2, the electrical part of the resonant gate transistor (RGT) which consists of the channel region and source/drain has been described. In the fabrication of RGT, the electrical part has to be developed before creating the overlying bridge structure above the channel. The modal behaviour of the bridge structures have been studied in Chapter 4. The antinodes of the lowest symmetrical mode for the straight (aluminium and tantalum) and buckled (tantalum) bridges have been found to be around the middle position of the bridge length. Thus, the channel of RGT has been decided to be placed around the central position of the bridge length.

In Chapters 5-6, the *n*-channel metal-oxide-semiconductor field-effect transistor (*n*-MOSFET) and *n*-channel resonant gate transistor (*n*-RGT) will be developed. In Chapter 5, the fabrication parameters for the *n*-MOSFET will be designed and in Chapter 6 the designed parameters will be used to develop the *n*-RGT. The *n*-MOSFETs are fabricated and characterised in order to investigate the influence of the air gap spacing between the bridge gate and *n*-type channel region on the threshold voltage and transconductance of *n*-RGT.

In this chapter, the fabrication process for the enhancement and depletion mode *n*-MOSFETs will be presented and the fabrication parameters will be simulated in

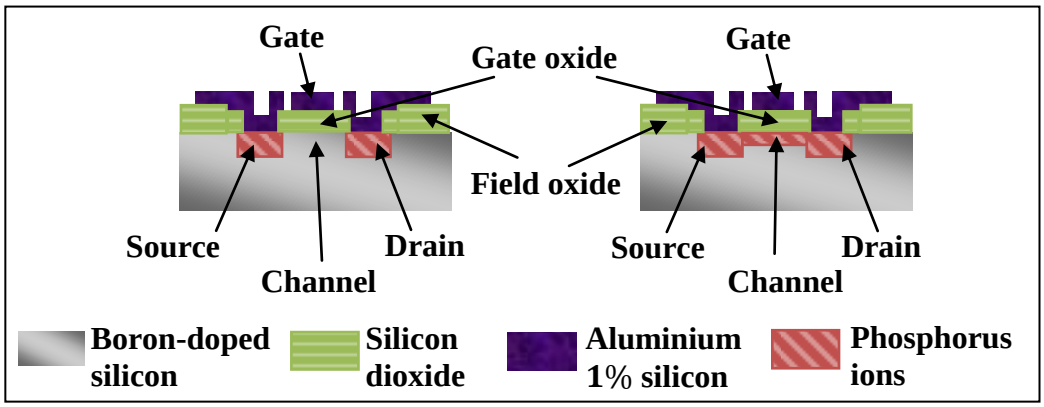
order to design the 1) threshold voltage for channel and 2) sheet resistivity for source/drain. Then, the channel and source/drain will be characterised using these 3 test structures, 1) the phosphorus implanted silicon test wafer, 2) Greek cross structure and 3) Kelvin resistor structure. The silicon test wafers will be implanted with phosphorus ions according to the simulated fabrication parameters and then measured using secondary ion mass spectrometry (SIMS) technique in order to characterise the 1) surface concentration of the depletion mode channel that quantifies the threshold voltage and 2) surface concentration and junction depth of the source/drain regions that quantify the sheet resistivity. The SIMS measurement error has reduced the accuracy of the junction depth characterisation. Thus, Greek cross structures will be used to measure directly the sheet resistivity of the source/drain regions. Finally, Kelvin resistor structures will be employed to measure and design the resistance of metal contact to source/drain. Reasonable sheet and contact resistivities for the source/drain regions are pursued.

5.2 Enhancement and depletion mode *n*-MOSFET

The cross sectional views of the *n*-MOSFET in enhancement and depletion mode are shown in Figure 5.1 [85]. Mainly, the device consists of the field oxide, gate oxide, channel, gate and source/drain terminals. In our study, aluminium 1% silicon has been employed as the conductive gate and metal contacts for source/drain. The heavily doped phosphorus ion regions have been implanted into the lightly boron-doped silicon substrate to create the source/drain regions. The channel is insulated from gate by a thin silicon dioxide layer (SiO_2) called the gate oxide. Generally, the gate, source/drain, gate oxide and channel are considered as the active region of *n*-MOSFET in which the transistor operation occurs. Field oxide is also an insulating SiO_2 layer which is grown to be $\sim$15 times thicker than the gate oxide. Field oxide does not involve in the transistor action (passive region) and serves primarily to prevent the conduction between active regions [48].

The MOSFET has similar operation with RGT as described in section 2.4.4. DC voltage V_{gs} is applied onto the gate in order to induce the formation of inversion layer

within the channel and to modulate the channel conductance. Then, the DC voltage between source and drain V_{ds} is applied in order to induce the electrical current I_{ds} to flow from drain to source [85]. The enhancement mode *n*-MOSFET [Figure 5.1(a)] requires V_{gs} to be higher than the threshold voltage, V_{th} in order for the current conduction to occur. Thus, the device is normally off and requires $V_{gs} > V_{th}$ to be turned on. In depletion mode *n*-MOSFET, the lightly doped phosphorus ion conducting channel is implanted between the source and drain [Figure 5.1(b)]. V_{gs} is applied to modulate the built-in channel conductance [85]. The device is normally on and requires $V_{gs} < V_{th}$ to be turned off.



(a) Enhancement mode **(b)** Depletion mode

Figure 5.1 *The cross sectional view of the (a) enhancement mode and (b) depletion mode n-MOSFET.*

5.3 The fabrication process

The fabrication steps are presented for the enhancement mode [Figure 5.2] and depletion mode [Figure 5.3] *n*-MOSFET. A 3-inch boron-doped $< 100 >$ silicon wafer with an average bulk resistivity of $17\ \Omega cm$ (nominal resistivity of $\rho = 14\ \Omega cm - 20\ \Omega cm$) has been used as the substrate body. The average concentration of boron within the silicon wafer is estimated to be $N_A \sim 8e^{14}\ atoms/cm^3$.

In Figure 5.2(a)(i), the silicon wafer is placed inside the furnace and SiO_2 field oxide layer of $0.5\ \mu m$ thickness has been thermally grown onto the silicon substrate. The reactive ion etching (RIE) has been performed on the field oxide in Plasmatherm

PK2440 RIE etcher using CF_4/H_2 plasma [Figure 5.2(b)(ii)]. This step defines the active region of the device. Etch time of $33\ minutes$ is required to pattern the $0.5\ \mu m$ of SiO_2. At this stage, the depletion mode *n*-MOSFET can be created by patterning the wafer photolithographically with SPR 350 photoresist of $1\ \mu m$ thickness in order to define the channel area and then implanting the phosphorus ions into silicon [Figure 5.3 (b)(ii)]. The photoresist will act as the masking layer during the implantation process. If no implantation of the channel involves at this point, the fabricated device will become the enhancement mode *n*-MOSFET. After the ion implantation step, the photoresist masking layer has been removed totally from the substrate in oxygen plasma for $1\ hour$. The subsequent processing steps will be the same for both enhancement and depletion mode *n*-MOSFET.

Next in Figure 5.2(c)(iii), the wafer has been patterned photolithographically in order to define the source and drain areas. The phosphorus ions have been implanted into the silicon substrate to create the source/drain regions. The parameters for the phosphorus ion implantation process i.e. ion beam dose and energy for both depletion mode channel and source/drain will be designed in sections 5.4.2 and 5.4.3. Then, the wafer has been annealed at $1100\ ℃$ for $30\ minutes$ in order for the implanted phosphorus ions within the substrate to be activated electrically [93]. After the activation step, a thin layer of gate oxide with $\sim 70\ nm$ thickness has been grown thermally using the dry oxidation process at $1100\ ℃$ for $30\ minutes$ [Figure 5.2(d)(iv)]. The implanted source/drain regions need to be in contact with the metal electrode pads through the pre-defined contact windows. In order to create the contact window, the wafer has been patterned photolithographically and RIE using CF_4/H_2 plasma has been performed on the gate oxide [Figure 5.2(e)(v)]. Etch time of $5\ minutes$ is required to pattern $70\ nm$ of SiO_2 gate oxide.

After removing the photoresist mask in oxygen plasma, aluminium 1 % silicon has been sputter-deposited onto the substrate as the metalisation layer. Aluminium 1 % silicon has been used instead of aluminium in order to prevent the silicon-to-aluminium solid state diffusion process from occurring at the source/drain regions.

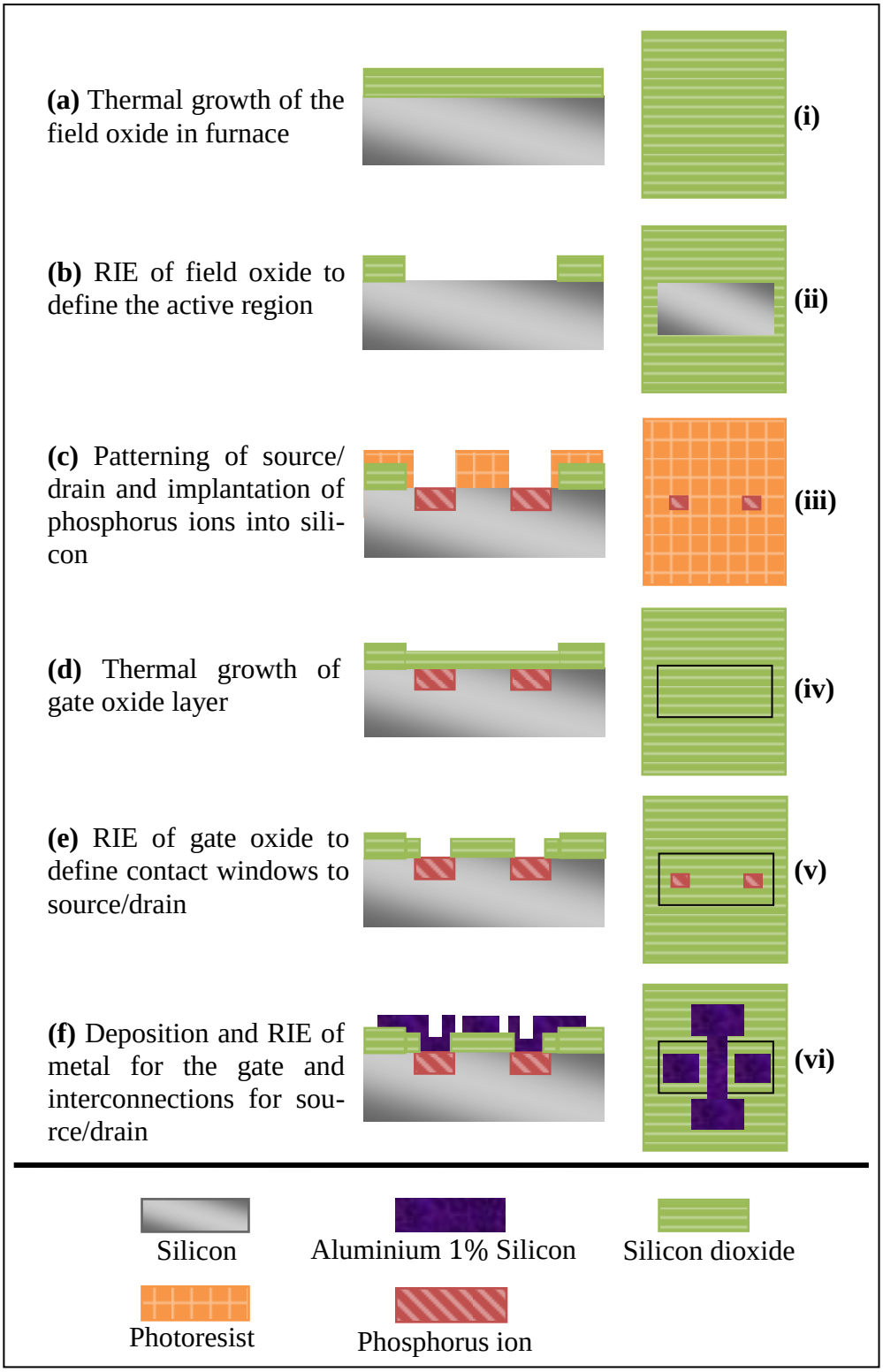


Figure 5.2 *The fabrication steps for making the enhancement mode n-MOSFET. [(a)-(f)] Cross sectional view of the process and [(i)-(vi)] top view of the process.*

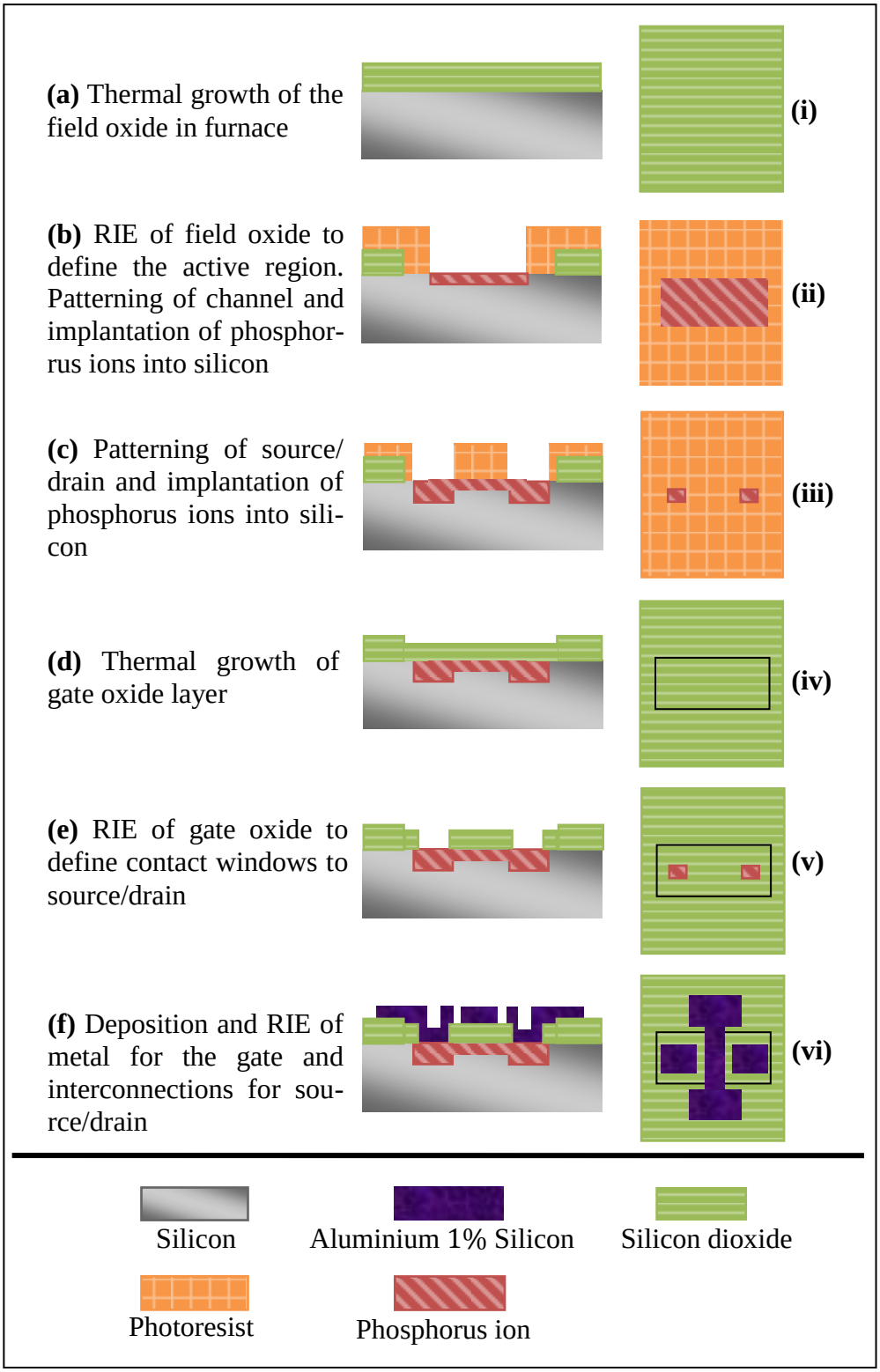


Figure 5.3 *The fabrication steps for making the depletion mode n-MOSFET. [(a)-(f)] Cross sectional view of the process and [(i)-(vi)] top view of the process.*

The silicon from substrate tends to migrate into the on-deposited aluminium leaving voids and then aluminium will migrate to fill in the voids, causing metal spikes into the substrate and junction shorts [94]. Addition of 1 % silicon helps to minimise the migration process [94].

Aluminium 1% silicon layer of 0.5 μm thickness has been sputter-deposited onto the wafer using the Balzers. The metal layer has been patterned photolithographically in order to define 1) the gate and 2) the metal electrode pads that will come in contact with the implanted source/drain regions [Figure 5.2(f)(iv)]. Aluminium 1% silicon has been etched using RIE employing $SiCl_4$/Ar plasma for 20 $minutes$ in STS metal etcher. After removing the photoresist mask in oxygen plasma, the wafer is annealed at 450 ℃ for 30 $minutes$ in order to lower the contact resistance between the aluminium 1% silicon metal and the phosphorus implanted source/drain regions.

5.4 The fabrication design for channel and source/drain of *n*-MOSFET

In this section, the fabrication design for channel and source/drain of the *n*-MOSFET has been studied. The fabrication parameters for enhancement mode channel (i.e. gate oxide thickness) and depletion mode channel (i.e. gate oxide thickness, ion beam dose and energy) will be simulated in order to design the threshold voltage. For source/drain, the fabrication parameters for implantation (i.e. ion beam dose and energy) will be simulated in order to design the sheet resistivity. The influence of temperature on dopants distribution within the channel and source/drain will be discussed. *TSUPREM-4* will be used to assist the design process.

5.4.1 Threshold voltage for enhancement mode channel

In enhancement mode *n*-MOSFET, the majority carriers within the silicon channel surface from the *p*-type body (boron doped substrate) are holes. A positive bias voltage V_{gs} applied onto the gate will repel the holes and attract the minority carriers i.e. electrons towards the channel. At threshold voltage, the induced electrons within the channel possess a concentration that exceeds the hole concentration [85]. The

channel has been changed from *p*-type to *n*-type and the induced electrons inversion layer connects the drain to source. Thus, the threshold voltage is a critical parameter that specifies minimum gate voltage needed to be applied in order to invert the silicon channel surface from *p*-type to *n*-type and obtain the drain current conduction.

Analytically, the threshold voltage for enhancement mode *n*-MOSFET depends on four factors 1) the boron doping concentration N_A at the silicon channel surface, 2) the presence of positive oxide charges Q_{ss} within the gate oxide, 3) the work function of the material used for the gate and 4) the distance of the silicon channel surface from metal gate i.e. the thickness of gate oxide t_{ox}. If the source and substrate body of the device are grounded, the threshold voltage of the enhancement mode *n*-MOSFET can be simplified into equation 5.1 [85][86];

$$V_{th} \approx 2\varphi_f + \frac{Q_B}{C_{ox}} + \varphi_{MS} - \frac{Q_{ss}}{C_{ox}} \tag{5.1}$$

where φ_{MS} is the work function difference between the metal gate and silicon channel, φ_f is the equilibrium electrostatic potential within the semiconductor, Q_B is the total charge stored per unit area within the ionised depletion region, C_{ox} is the gate oxide capacitance per unit area and finally Q_{ss} is the total positive oxide charges per unit area [85][86]. For the *p*-type semiconductor body, φ_f is given by equation 5.2 where $V_t = 25.9\,mV$ at $300\,K$ and η_i is the intrinsic carrier concentration of the semiconductor body i.e. silicon [85][86];

$$\varphi_f = V_t \ln\left(\frac{N_A}{\eta_i}\right) \tag{5.2}$$

Using aluminium 1% silicon as the gate, the value of φ_{MS} has been assumed to be $-0.82\,eV$. The value of gate oxide capacitance per unit area is determined from $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ with ε_{ox} and t_{ox} being the permittivity and thickness of the gate oxide. Then, Q_B is found from equation 5.3 with ε_{si} being the permittivity of the silicon substrate and $q = 1.6e^{-19}\,C$ [85][86].

$$Q_B = \sqrt{2\varepsilon_{si} q N_A \left|-2\varphi_f\right|} \tag{5.3}$$

Typical values of $Q_{ss} = q(2 - 3e^{11})\ cm^{-2}$ have been measured by others from a thermally grown gate oxide [87]. In our design, $Q_{ss} = q(3e^{11})cm^{-2}$ has been assumed.

The targeted threshold voltage range for the enhancement mode channel is within $0\ V$ to $1\ V$. From simulation in *TSUPREM-4*, the influence of increasing the gate oxide thickness t_{ox} has been seen to increase the threshold voltage. In addition, the presence of Q_{ss} within gate oxide has made the positive threshold voltage to become negative and the negative threshold voltage increases with the increase of Q_{ss}. This implies that the device will be conducting at zero gate voltage V_{gs}, behaving like a depletion mode *n*-MOSFET instead of the enhancement mode. The trapped Q_{ss} located close to the gate oxide-silicon channel interface has been suspected to induce the formation of electrons inversion layer in the absence of any applied gate voltage, resulting in the depletion type characteristics of the channel [87]. Therefore, due to the presence of $Q_{ss} = q(3e^{11})cm^{-2}$, the designed threshold voltage for the enhancement mode channel of t_{ox}~$70\ nm$ has been simulated to be $-1.1\ V$. In Chapter 6, the fabricated enhancement mode *n*-MOSFET with the designed t_{ox}~$70\ nm$ has been measured to have V_{th}~$-\ 1.2\ V$, verifying the presence of Q_{ss} within the gate oxide.

5.4.1.1 Influence of high temperature on boron concentration

The channel doping profile for the enhancement mode *n*-MOSFET after the growth of ~$70\ nm$ gate oxide is simulated in Figure 5.4 with the simulated threshold voltage of $V_{th} = -1.1\ V$. The channel doping profile plots the concentration of boron within the gate oxide and with respect to the depth of silicon substrate. The annealing step for the phosphorus implantation regions, the field oxidation and gate oxidation processes have been simulated to reduce the concentration of boron at the silicon channel surface. The dopant segregation effect can occur at the gate oxide-silicon channel interface in which boron dopants near the silicon channel surface redistributed themselves at high temperature processes [85]. Segregation happens due to boron having different concentration at equilibrium in different materials, in

this case in silicon dioxide and silicon. Thus, boron in silicon segregates into silicon dioxide, leaving the silicon channel surface to be depleted of boron. The concentration of boron N_A at the silicon channel surface has been described to affect the threshold voltage. For the fabrication of enhancement mode *n*-MOSFET using lower temperature processes, N_A has been simulated to be higher while the negative threshold voltage becomes smaller.

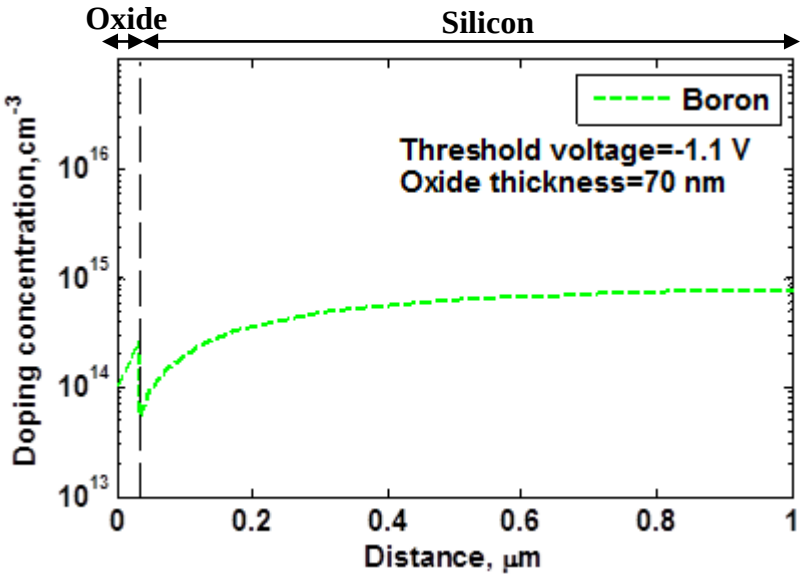


Figure 5.4 *The channel doping profile of the enhancement mode n-MOSFET with the simulated threshold voltage $V_{th} = -1.1\,V$ and gate oxide thickness $t_{ox} = 70\,nm$. Boron concentration at the silicon channel surface has been simulated to decrease at high temperature process.*

5.4.2 Threshold voltage for depletion mode channel

The targeted threshold voltage range for the depletion mode channel is within $-1\,V$ to $-3\,V$. In depletion mode *n*-MOSFET, a lightly phosphorus-doped conducting channel is created between source and drain by ion implantation technique. The technique introduces phosphorus ions into the silicon wafer using high energy beam [48]. The energy and dose of the phosphorus ion beam have to be specified for the implantation procedure.

The threshold voltage of the depletion mode channel has been simulated to be $V_{th} = -1.58\,V$ using the phosphorus ion beam of dose $= 8e^{11}\ ions/cm^2$ and energy

$= 40\ keV$, implanted into the boron-doped silicon. The channel doping profile in Figure 5.5 shows the distribution of phosphorus and boron dopants after the growth of $\sim 70\ nm$ gate oxide.

The junction depth is defined as the depth at which the phosphorus concentration equals to the boron concentration i.e. the distance from the silicon channel surface to the PN junction [Figure 5.5]. The junction depth is an important parameter for the design of sheet resistivity of the source/drain implantation regions which will be discussed in section 5.4.3.1.

For channel implantation, the important parameter is the surface concentration of phosphorus dopants N_D that determines the magnitude of the threshold voltage. In Figure 5.5, the phosphorus ion implantation of dose $= 8e^{11}\ ions/cm^2$ and energy $= 40\ keV$ has simulated $N_D = 3.0e^{15}\ cm^{-3}$ which gives $V_{th} = -1.58\ V$. In addition, the concentration of phosphorus at the silicon channel surface has not been reduced by the high temperature processes during the source/drain annealing step and gate oxidation.

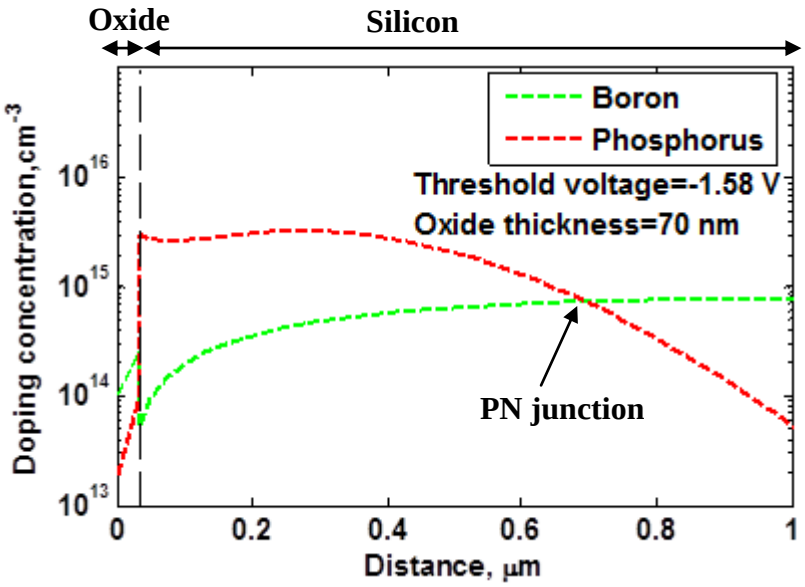


Figure 5.5 *The channel doping profile of the depletion mode n-MOSFET with the simulated threshold voltage $V_{th} = -1.58\ V$ and gate oxide thickness $t_{ox} = 70\ nm$. The surface concentration of phosphorus dopants $N_D = 3.0e^{15} cm^{-3}$ gives $V_{th} = -1.58\ V$.*

5.4.2.1 Design of surface concentration N_D

For depletion mode channel implantation, phosphorus doses of $8e^{11}\ ions/cm^2$ and $2e^{12}\ ions/cm^2$ with energies ranging from 30 keV to 50 keV have been considered for the simulation of phosphorus surface concentration N_D and the corresponding threshold voltage V_{th}. The simulation result in Table 5.1 shows that higher ion beam dose and energy increase the phosphorus surface concentration and thus, increases the negative threshold voltage of the depletion mode *n*-MOSFET.

Therefore, the phosphorus doses of $8e^{11}\ ions/cm^2 - 2e^{12}\ ions/cm^2$ with energies of $30\ keV - 50\ keV$ can be used for the implantation process in order to fabricate the depletion mode *n*-MOSFET devices with the threshold voltage range from $-3\ V$ to $-1\ V$ at t_{ox}~$70\ nm$. In this chapter, the phosphorus surface concentration N_D of the depletion mode channel will be measured using SIMS technique while the measurement and characterisation of the threshold voltage for the depletion mode *n*-MOSFET devices will be presented in Chapter 6.

Dose $(ions/cm^2)$	Energy (keV)	N_D (cm^{-3})	V_{th} (V)
$8e^{11}$	30	$2.5e^{15}$	-1.47
$8e^{11}$	40	$3.0e^{15}$	-1.58
$8e^{11}$	50	$3.5e^{15}$	-1.67
$2e^{12}$	30	$6.0e^{15}$	-2.30
$2e^{12}$	40	$7.0e^{15}$	-2.54
$2e^{12}$	50	$8.0e^{15}$	-2.76

Table 5.1 *Design of N_D with respect to dose and energy of the phosphorus ion beam that quantifies V_{th} for the depletion mode n-MOSFET.*

5.4.3 Sheet resistivity for source/drain implantation regions

In this section, the ion beam dose and energy will be designed in order to simulate the sheet resistivity of the phosphorus implanted source/drain regions. Normally, high implant doses are required for source/drain in order for these regions to possess

small resistances. Common dose values for source/drain are within $\sim 10^{15} - \sim 10^{16}\ ions/cm^2$ range which is $\sim 4 - 5$ orders of magnitude higher than the doses used for depletion mode channel [48][85][92]. The sheet resistivity ρ_s of the implanted region is determined by the distribution of the phosphorus surface concentration N_D with the junction depth X_j [48]. ρ_s of $13\ \Omega/\square - 53\ \Omega/\square$ range have been measured for phosphorus and arsenic implanted source/drain regions [92]. Small sheet resistivity for source/drain implantation regions is necessary in order to achieve high drain current conduction within the *n*-MOSFET devices.

Dose $(ions/cm^2)$	Energy (keV)	N_D (cm^{-3})	X_j (μm)	ρ_s $(\Omega/\square)$
$1e^{14}$	20	$3.0e^{17}$	1.14	870.36
$1e^{14}$	30	$4.0e^{17}$	1.16	754.85
$1e^{14}$	40	$5.0e^{17}$	1.19	683.46
$1e^{15}$	20	$3.5e^{18}$	1.36	201.01
$1e^{15}$	30	$4.5e^{18}$	1.39	178.28
$1e^{15}$	40	$5.5e^{18}$	1.40	174.51
$1e^{16}$	20	$4.0e^{19}$	1.92	22.64
$1e^{16}$	30	$5.5e^{19}$	1.97	21.00
$1e^{16}$	40	$6.5e^{19}$	1.99	20.40

Table 5.2 *Design of N_D and X_j with respect to dose and energy of phosphorus ion beam that quantifies ρ_s for the source/drain regions.*

5.4.3.1 Design of surface concentration N_D and junction depth X_j

For source/drain ions implantation, phosphorus doses of $1e^{14}\ ions/cm^2$ to $1e^{16}\ ions/cm^2$ and energies ranging from $20\ keV$ to $40\ keV$ have been considered for the simulation of phosphorus surface concentration N_D and junction depth X_j which will determine the sheet resistivity ρ_s. The simulation result in Table 5.2 shows that higher ion beam dose and energy increase the phosphorus surface concentration and junction depth. The increase in phosphorus surface concentration

with respect to the increase in ion beam energy has been found to be due to the high temperature processes during the fabrication of *n*-MOSFET devices. The effect of increase in junction depth is more dominant than the effect of increase in phosphorus surface concentration and thus, decreases the sheet resistivity of the phosphorus implanted source/drain regions.

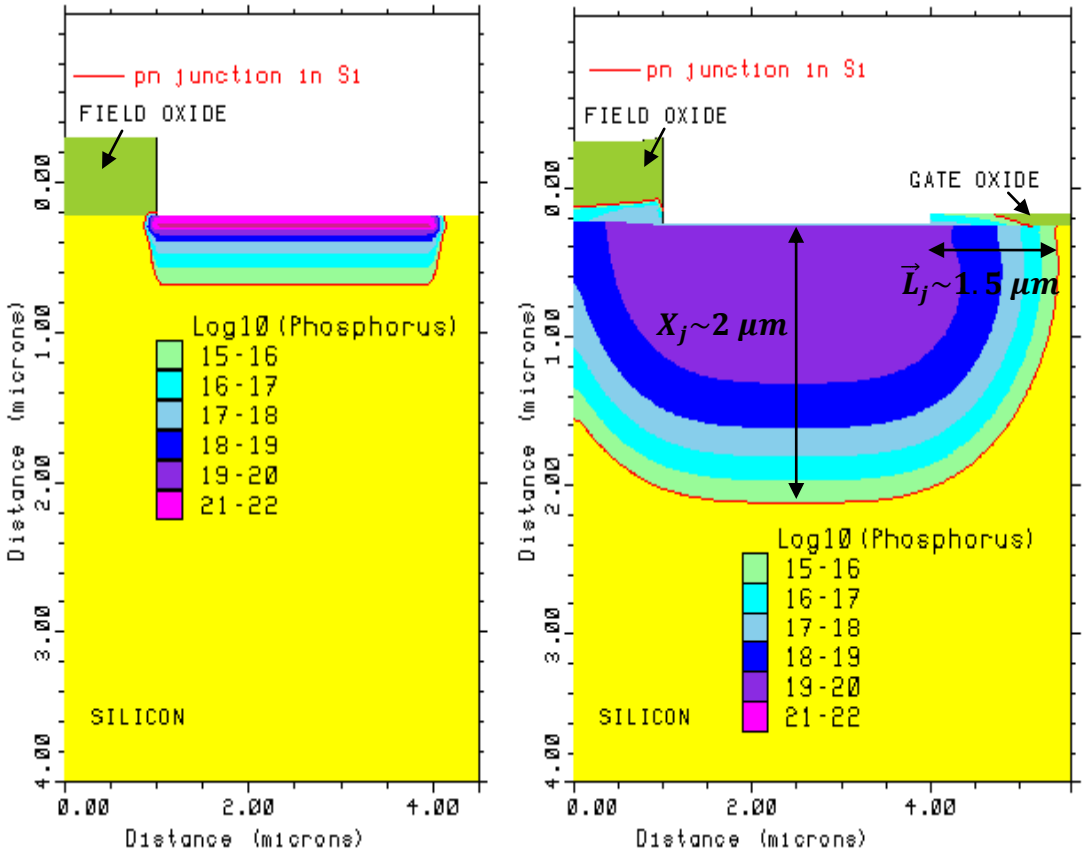
From Table 5.2, the phosphorus dose of $1e^{16}\ ions/cm^2$ with energy of $40\ keV$ will be used in the source/drain implantation process in order to obtain reasonably small sheet resistivity of $20.4\ \Omega/\square$. In this chapter, the phosphorus surface concentration N_D and junction depth X_j of source/drain will be measured using SIMS technique in order to quantify ρ_s. In addition, direct measurement of ρ_s for source/drain will be conducted using Greek cross test structure.

5.4.3.2 Influence of temperature on channel length

Previously, the influence of high temperature processes has been simulated to cause the boron segregation effect to occur within the enhancement mode channel that changes the boron surface concentration and thus changes the threshold voltage. For the phosphorus implanted source/drain regions, the annealing step after phosphorus implantation and the growth of gate oxide have been simulated to change the distribution profile of the phosphorus dopants. Figure 5.6 shows the two-dimensional simulation profiles of the implanted phosphorus ions in source/drain regions before and after being subjected to the gate oxidation and implantation annealing processes. High furnace temperatures in these two processes have been simulated to cause the implanted phosphorus ions to diffuse laterally and vertically, giving the junction depth of $X_j{\sim}2\ \mu m$ for phosphorus dose of $1e^{16}\ ions/cm^2$ and energy of $40\ keV$ [Figure 5.6(b)]. The lateral diffusion length under the gate oxide is $\vec{L}_j{\sim}1.5\ \mu m$.

The source/drain phosphorus lateral diffusion can affect the channel length L_c of the *n*-MOSFET. The effective channel length of the device will be smaller than its initial designed value and consequently, short channel effects can occur within the

device. At the considered gate oxidation and implantation annealing processes, $\vec{L}_j \sim 1.5\ \mu m$ from both source and drain implanted regions will make the effective channel length to be $\sim 3\ \mu m$ smaller than the initial designed value. Short channel effects might not be a major problem for the designed L_c of $10\ \mu m - 30\ \mu m$ range, giving the effective channel length to be $\sim 7\ \mu m - 27\ \mu m$.



(a) Before heat treatment **(b)** After heat treatment

Figure 5.6 *Simulation of source/drain doping profile (a) before and (b) after the implantation annealing and gate oxidation processes. The high temperature processes caused vertical and lateral diffusion of the implanted phosphorus dopants.*

5.5 The measurement and characterisation for depletion mode channel and source/drain of *n*-MOSFET

In this section, the fabrication design from section 5.4 will be used to characterise the depletion mode channel and source/drain of *n*-MOSFET. The simulated ion beam dose and energy for the depletion mode channel will be employed and the

corresponding phosphorus surface concentration N_D will be measured. The measurement has been performed using the secondary ion mass spectrometry (SIMS) technique on the phosphorus implanted silicon test wafer. The measurement of N_D will verify the designed fabrication parameters in *TSUPREM-4*.

Similarly, the phosphorus surface concentration N_D and junction depth X_j for the phosphorus implanted source/drain regions will be measured using SIMS technique in order to verify the designed ion beam dose and energy and to quantify the sheet resistivity ρ_s. Alternatively, ρ_s will be measured directly using the Greek cross test structures. The investigation continues with the measurement of the contact resistivity between the aluminium 1 % silicon metalisation layer and the phosphorus implanted source/drain regions using the Kelvin resistor test structure. The fabrication design for the metal contact has been optimised in order to obtain reasonable values of contact resistivity.

5.5.1 Measurement of N_D and X_j for depletion mode channel and source/drain

The 3-inch $< 100 >$ boron-doped silicon wafer has been employed as the test wafer. The wafer has been measured in the automatic 4-point probe station and the average bulk resistivity of the substrate is $\rho \sim 17\ \Omega cm$. Thus, the concentration of boron dopant within the wafer has been taken to be $N_A \sim 8e^{14}\ atoms/cm^3$. Then, the phosphorus ions have been implanted into the wafer. The implantation process has been carried out by Ion Beam Services (IBS).

In order to fabricate the depletion mode *n*-MOSFETs with the threshold voltage range of $-3\ V$ to $-1\ V$ at gate oxide thickness of $t_{ox} \sim 70\ nm$, phosphorus ion doses of $8e^{11}\ ions/cm^2 - 2e^{12}\ ions/cm^2$ with the energies within $30\ keV - 50\ keV$ range have been targeted for the depletion mode channel implantation process. In this study, two test wafers have been implanted with dose/energy of $8e^{11}/40$ and $2e^{12}/40$, respectively and the corresponding phosphorus surface concentration N_D has been measured. The threshold voltages for the fabricated depletion mode *n*-MOSFETs in Chapter 6 have been measured to be within $-3\ V$ to $-1\ V$. For the

implantation of source/drain, phosphorus dose of $1e^{16}\ ions/cm^2$ with $40\ keV$ energy has been targeted in order to obtain the sheet resistivity of $20.4\ \Omega/\square$. Therefore, one test wafer has been implanted with dose/energy of $1e^{16}/40$ and the phosphorus surface concentration N_D and junction depth X_j have been measured.

All three phosphorus implanted silicon test wafers have been annealed at 1100 ℃ for $30\ minutes$ in order to activate the phosphorus ions. The influence of temperature from the gate oxidation process is included in the experiment. Then, the doping profiles of the phosphorus implanted silicon test wafers have been inspected using the secondary ion mass spectrometry (SIMS).

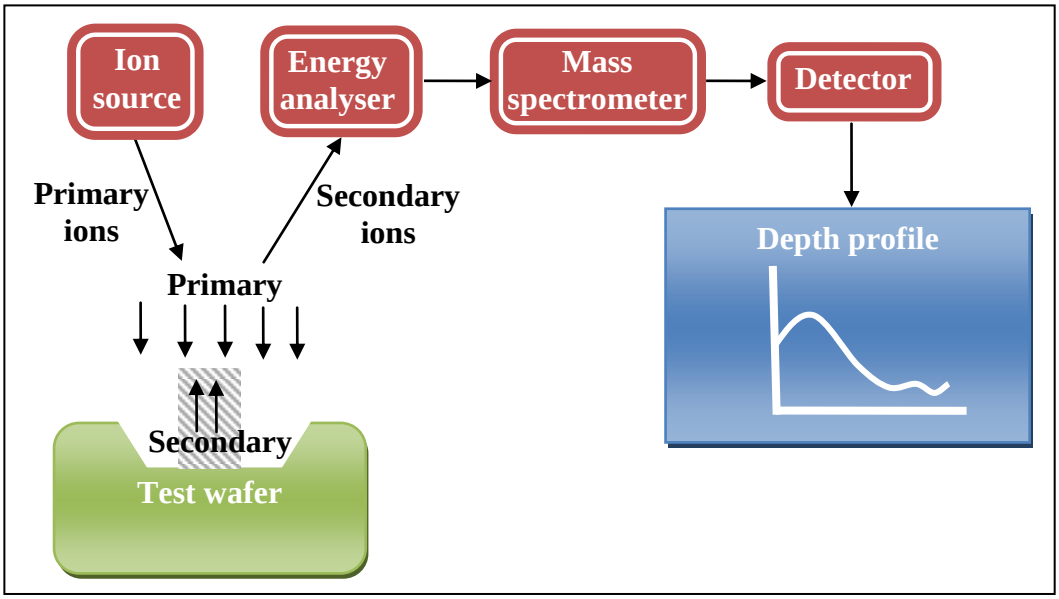


Figure 5.7 *Block diagram of SIMS technique for depth profiling of the dopant within semiconductor [91].*

5.5.1.1 Secondary ion mass spectrometry (SIMS)

The block diagram in Figure 5.7 summarises the operation of SIMS technique for semiconductor dopant profiling method [91]. The technique employs the primary focused beam of high energy caesium ions Cs^+onto the phosphorus implanted silicon test wafers, producing secondary particles of phosphorus ions P^- that are detected by the mass spectrometer. A well-defined crater is produced on the silicon substrate when the primary beam is sputtered over a rectangular area on the test wafer. The

secondary ions are detected at a smaller area within the crater. The concentration of the implanted phosphorus ions with respect to depth within the boron-doped silicon substrate is then obtained.

5.5.1.2 Doping profile measurement

The measured doping profiles for the depletion mode channel and source/drain are plotted in Figure 5.8 and compared with the simulation results. The measured phosphorus surface concentrations N_D agree well with the simulations. Therefore, $N_D{\sim}3e^{15}\ atoms/cm^3$ and $N_D{\sim}7e^{15}\ atoms/cm^3$ for depletion mode channel can be achieved by employing dose/energy of $8e^{11}/40$ and $2e^{12}/40$, respectively. Similarly, $N_D{\sim}6e^{19} atoms/cm^3$ for the source/drain implantation regions is obtained with dose/energy of $1e^{16}/40$.

In Figure 5.8, the measured junction depths X_j are bigger than the simulated values. There are two reasons that might explain this discrepancy. First, the phosphorus ion channelling effect might have occurred along the crystal planes in silicon. Thus, the phosphorus ion penetration is enhanced making the junction depth to be deeper than expected. From simulation, the phosphorus channelling effect in $< 100 >$ silicon wafer as a function of ion beam tilt and twist angle has not been included. Thus, the body tails of the distribution curves from simulations are shallower than the profiles obtained from SIMS measurements.

Second, the secondary ions detection area has been made to be comparatively the same as the area of the crater. An accurate depth profiling method requires the area of the crater to be larger than the detection area in order to prevent the contribution of the phosphorus ions from the crater wall. The detected phosphorus ions from the crater wall can cause the measured junction depths to be deeper than their actual depth [91].

For the phosphorus implanted source/drain regions, the measured surface concentration of $N_D{\sim}6e^{19} atoms/cm^3$ can be used in conjunction with the measured junction depth to estimate the sheet resistivity of the implanted phosphorus regions.

Since the junction depth X_j could not be detected accurately from SIMS measurement, the sheet resistivity of the phosphorus implanted source/drain regions have been measured directly using the Greek cross test structures.

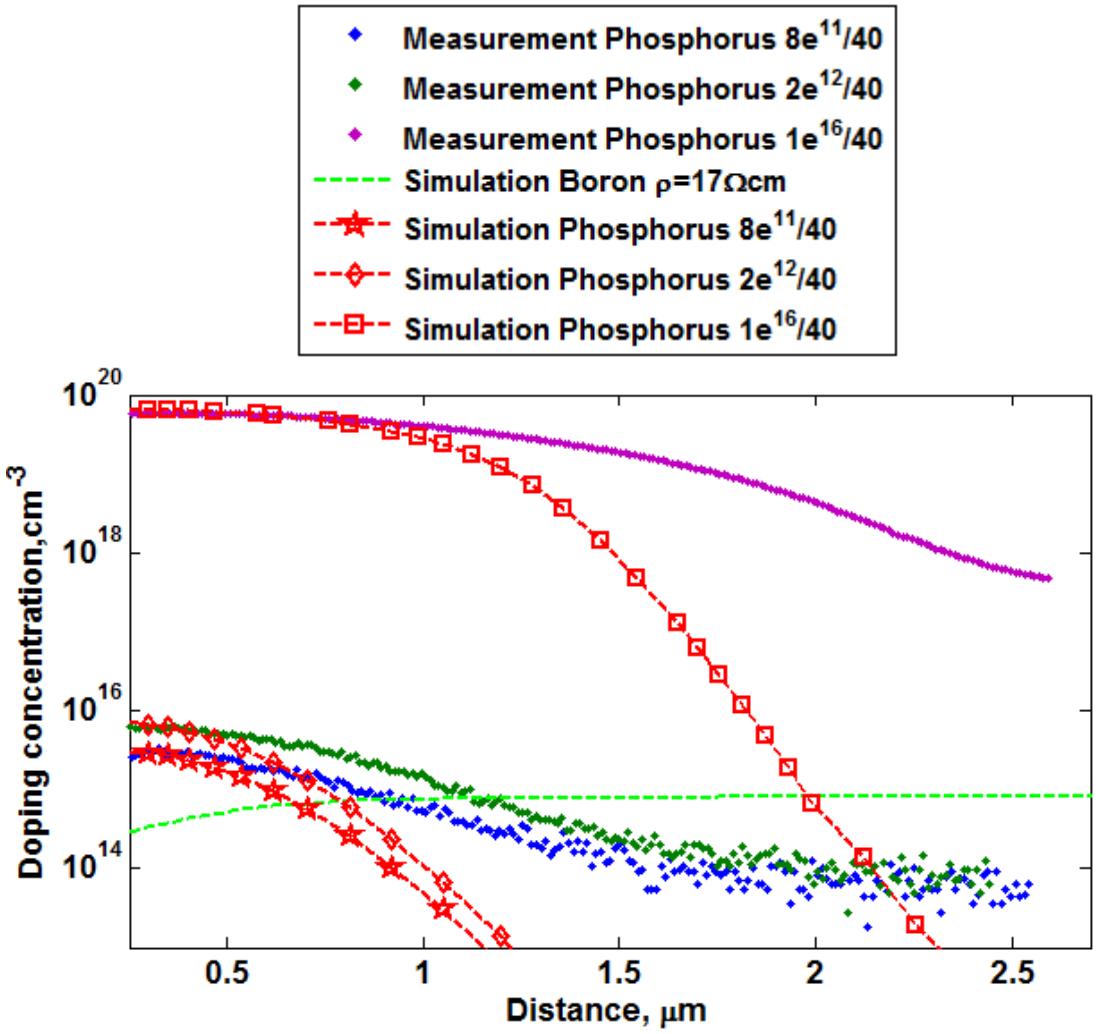


Figure 5.8 *Comparison between the measurement and simulation of the doping profiles for the depletion mode channel* ($8e^{11}/40$ *and* $2e^{12}/40$) *and source/drain implantation regions* ($1e^{16}/40$).

5.5.2 Measurement of sheet resistivity for source/drain

The phosphorus ion beam dose and energy for the implantation of the source/drain regions has been designed to be $1e^{16}\ ions/cm^2$ and 40 keV in order to obtain small sheet resistivity of 20.4 Ω/□. Therefore, the fabricated *n*-MOSFET devices can have

good drain current conductions with low resistances. The Greek cross test structure is a 4-point probing technique that can extract the sheet resistivity from a thin ion-implanted semiconductor layer or the thin film sputter-deposited metallic conductor layer [94]. The Greek cross structures only occupy small areas on the wafer and can be fabricated simultaneously with the *n*-MOSFET devices using the same fabrication steps. This provides an *in situ* sheet resistivity measurement for the phosphorus implanted source/drain regions of the *n*-MOSFET. In addition, the influence of temperature from the annealing step after implantation and gate oxidation process are included in the experiment. The fabricated Greek cross structures have also been distributed uniformly on the wafer in order to map the sheet resistivity of the phosphorus implantation across the wafer.

5.5.2.1 Fabrication of Greek cross test structure

The fabrication steps and geometrical dimensions of the Greek cross test structure are illustrated in Figure 5.9 and Figure 5.10. In Figure 5.9(a)(i), the silicon dioxide layer of $0.5\,\mu m$ thickness has been grown thermally on a 3-inch boron-doped $< 100 >$ silicon wafer with an average bulk resistivity of $17\,\Omega cm$. Then, in Figure 5.9(b)(ii), the wafer has been patterned photolithographically with the cross structure and RIE technique has been performed on the silicon dioxide layer using CF_4/H_2 plasma, revealing the regions for implantation. After removing the photoresist lithography mask in oxygen plasma, the silicon wafer substrate has been implanted with phosphorus ions of dose $= 1e^{16}\,ions/cm^2$ and energy $= 40\,keV$ [Figure 5.9(c)(iii)]. The annealing/activation step for the implanted phosphorus ions has been carried out at $1100\,℃$ for $30\,minutes$. A thin silicon dioxide passivation layer of $\sim 70\,nm$ thickness has been grown thermally on top of the implantation regions using the dry oxidation process at $1100\,℃$ for $30\,minutes$ [Figure 5.9(d)(iv)]. Next, the implanted phosphorus regions need to be in contact with the metal electrode pads. First, the metal to silicon contact windows have been patterned photolithographically on the wafer and RIE using CF_4/H_2 plasma has been performed on the passivation layer to create the contact windows [Figure 5.9(e)(v)]. Then, the

aluminium 1% silicon has been sputter-deposited onto the wafer as the metalisation layer and patterned photolithographically to define the electrodes [Figure 5.9(f)(vi)].

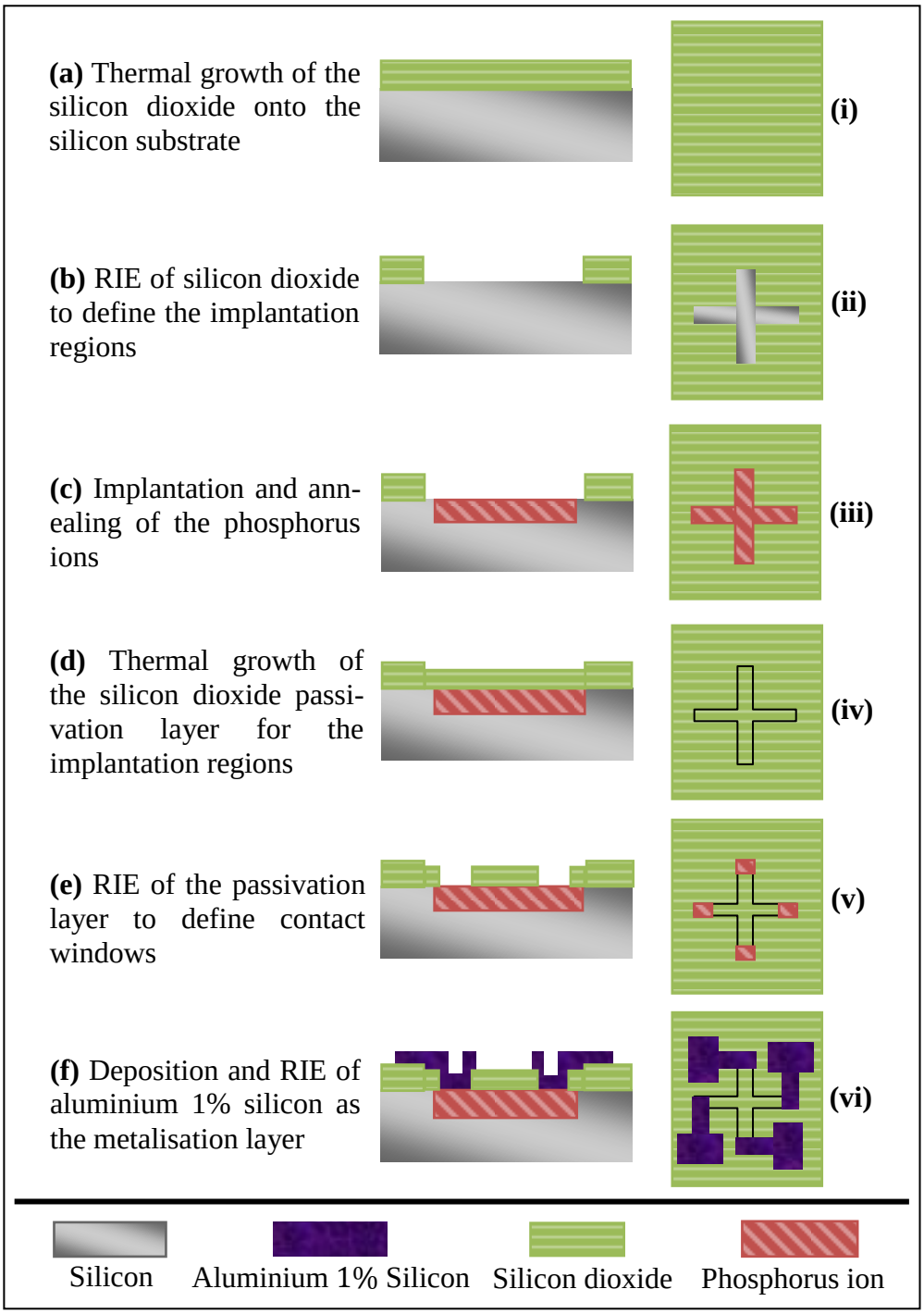
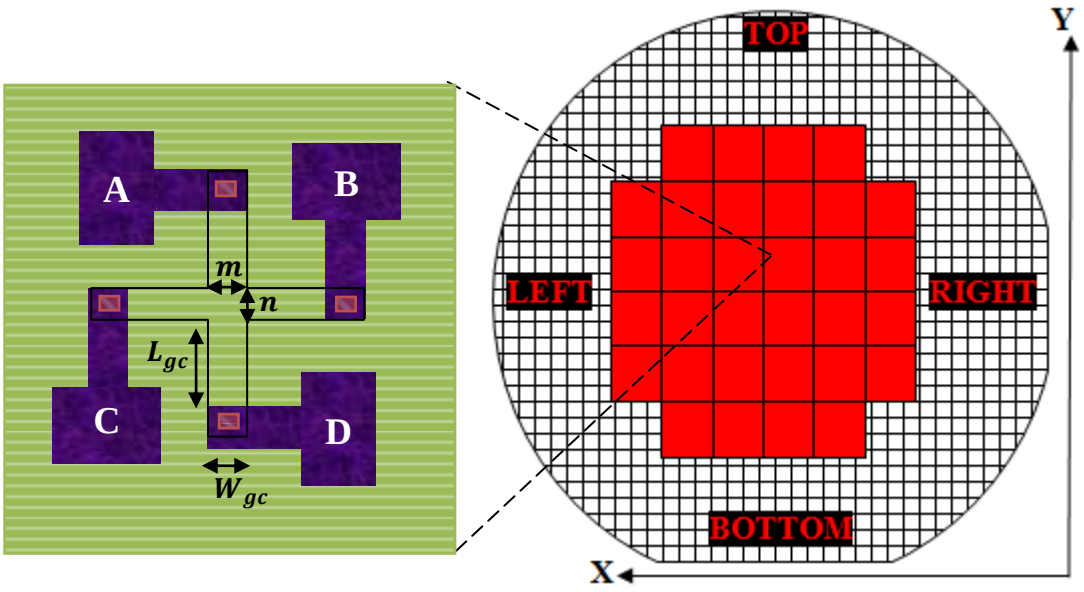


Figure 5.9 *The fabrication steps for making the Greek cross test structures. [(a)-(f)] The cross sectional view of the process and [(i)-(vi)] top view of the process.*

After removing the photoresist lithography mask, the wafer is annealed at 450 ℃ for 30 $minutes$ in order to lower the contact resistance between the aluminium 1% silicon metal electrodes and the implanted phosphorus regions. Finally, the fabricated Greek cross test structures have been probed electrically to measure the sheet resistivity of the implanted phosphorus regions.



(a) Greek cross **(b)** $<100>$ silicon wafer

Figure 5.10 *(a) The geometrical dimensions of the Greek cross test structure (b) The Greek cross test structures are distributed on 32 chips across the 3–inch boron-doped* $<100>$ *silicon wafer according to the X-Y coordinates.*

In Figure 5.10(a), the Greek cross test structures with arms length of $L_{gc} = 100\ \mu m$ and arms width of $W_{gc} = 5\ \mu m$, $8\ \mu m$, $10\ \mu m$ and $16\ \mu m$ have been fabricated. In Figure 5.10(b), the fabricated structures are shown to be distributed at 32 different chips across the whole wafer. The electrical measurement requires $L_{gc} > 2W_{gc}$ but the arms length should also be made as short as possible in order 1) to minimise the heat generation in the arms and 2) to prevent the surface leakage current [94][96]. In Figure 5.10(a), the extracted sheet resistivity of the implanted phosphorus ions is at the heart of the cross structure with the size of $m \times n$ [94][96].

5.5.2.2 Measurement of Greek cross test structure

The fabricated Greek cross test structures have been measured using the Hewlett Packard 4156B Semiconductor Parameter Analyzer. In this 4-point probe technique, two probes are used to carry the current and the remaining two probes are used for voltage sensing [94]. In Greek cross test structure shown in Figure 5.10(a), $50\ \mu A$ of drive current I_{AB} is passed between metal pad A and B and the corresponding potential difference between metal pad D and C is measured as V_{DC} [95][96]. The drive current must be kept below $0.1\ mA$ to prevent surface leakage current [94][96]. Higher measurement accuracy is achieved by reversing the current to I_{BA} and measure V_{CD}. The measured resistance R_{0° is given by equation 5.4. Similarly, the action is repeated for the drive current applied between metal pad B and C, giving the measured resistance R_{90° as in equation 5.5.

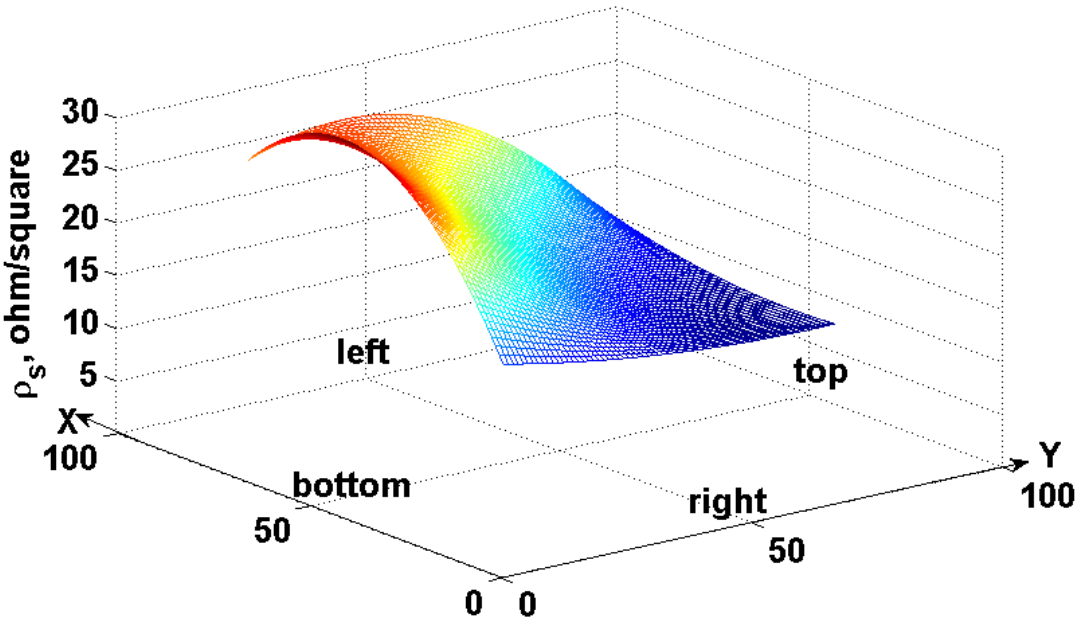
$$R_{0^\circ} = \frac{V_{DC} - V_{CD}}{I_{AB} - I_{BA}} \tag{5.4}$$

$$R_{90^\circ} = \frac{V_{AD} - V_{DA}}{I_{BC} - I_{CB}} \tag{5.5}$$

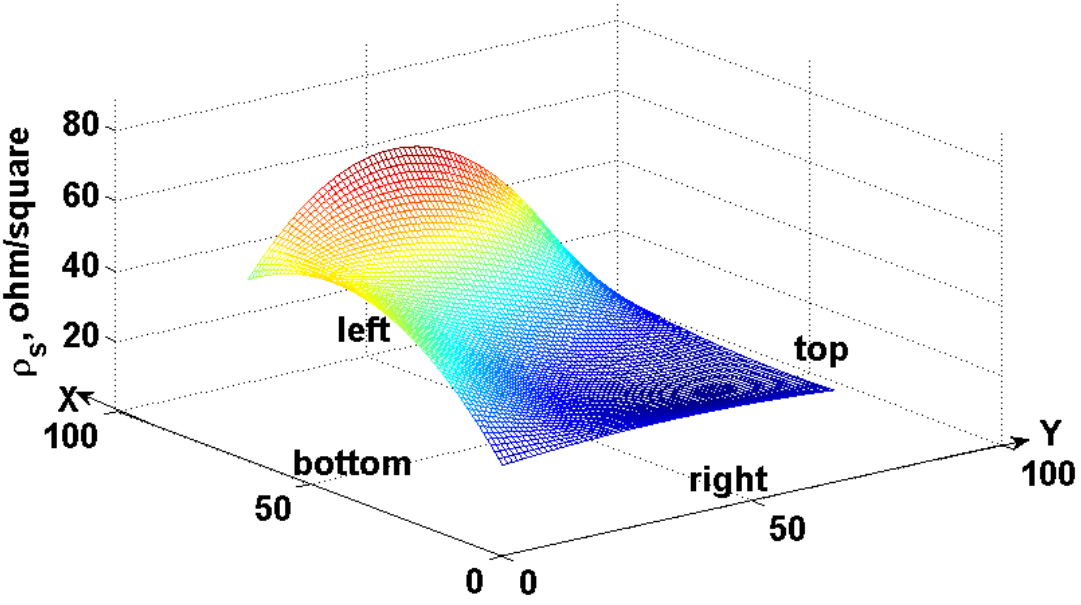
The average of the measured resistances is calculated as R_{ave} and finally, the sheet resistivity ρ_s is extracted as in equation 5.6;

$$\rho_s = \frac{\pi R_{ave}}{ln(2)} \tag{5.6}$$

In Figure 5.11, the sheet resistivities ρ_s of the implanted phosphorus ions have been measured and mapped with respect to the X-Y coordinates of the 3-inch boron-doped $< 100 >$ silicon wafer. The Greek cross test structures with the heart size of $16\ \mu m \times 16\ \mu m$ and $5\ \mu m \times 5\ \mu m$ have been considered. In both cases, the measured sheet resistivities of the implanted phosphorus ions have been observed to be non-uniform across the wafer. At the positions close to the bottom and left side of the wafer the sheet resistivities are approximately $2 - 3$ times higher in magnitude compared to the ones measured close to the top and right positions of the wafer.



(a) Heart size of 16 $\mu m \times 16\ \mu m$



(b) Heart size of 5 $\mu m \times 5\ \mu m$

Figure 5.11 *The non-uniform sheet resistivity profile of the implanted phosphorus ions measured with respect to the X-Y coordinates of the 3-inch boron-doped* $< 100 >$ *silicon wafer. The Greek cross test structures with heart size of (a)* 16 $\mu m \times 16\ \mu m$ *and (b)* 5 $\mu m \times 5\ \mu m$ *have been used.*

The variation in sheet resistivity measurement across the wafer might be due to the 1) non-uniform boron doping within the wafer substrate, 2) non-uniform phosphorus

ions implantation on the wafer or 3) error in measurement [94]. In our study, the phosphorus implantation process has been carried out in IBS with high uniformity across the whole wafer. Consistent probe spacings have been used during measurement and the averaging of several independent readings has reduced the measurement error to $\pm 0.4\ \Omega/\square$. Thus, the main reason for the variation in sheet resistivity measurement is due to the variation of boron concentration within the substrate.

5.5.2.3 Influence of heart size on sheet resistivity measurement

In Figure 5.11(a), the measured sheet resistivities from the Greek cross structures of heart size $16\ \mu m \times 16\ \mu m$ have been observed to be smaller compared to the measured sheet resistivities from the Greek cross structures of heart size $5\ \mu m \times 5\ \mu m$ in Figure 5.11(b). In Figure 5.12, the measured sheet resistivities from the Greek cross structures of heart size $5\ \mu m \times 5\ \mu m$, $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$ at five different positions across the wafer have been plotted. The average sheet resistivity of the implanted phosphorus ions across the wafer for $16\ \mu m \times 16\ \mu m$ is $\rho_s = 25.93\ \Omega/\square$. The decrease of heart size to $10\ \mu m \times 10\ \mu m$, $8\ \mu m \times 8\ \mu m$ and $5\ \mu m \times 5\ \mu m$ has increased the average sheet resistivity to $32.27\Omega/\square$, $44.14\ \Omega/\square$ and $52.21\ \Omega/\square$, respectively.

The applied drive current raises the temperature of the implanted phosphorus ions region at the arms and heart of the Greek cross test structure [94][96]. The heating increases the sheet resistivity of the implanted phosphorus region and this introduces error in the measurement. The heating can be minimised by decreasing the arm length L_{gc} or increasing the heart size $m \times n$ of the Greek cross test structure [96].

Thus, a more accurate sheet resistivity measurement with smaller heating effect has been obtained from the Greek cross test structure of heart size $16\ \mu m \times 16\ \mu m$. In conclusion, the average sheet resistivity of the phosphorus implanted source/drain regions using ion beam dose of $1e^{16}\ ions/cm^2$ and energy of $40\ keV$ has been measured to be $\rho_s = 25.93\ \Omega/\square$. The measured value is slightly higher than the

simulated value of $\rho_s = 20.4\,\Omega/\square$, probably due to the heating effect within the structure. The measured sheet resistivity for source/drain regions is considerably small and thus, good drain current conduction can be achieved from the *n*-MOSFET devices.

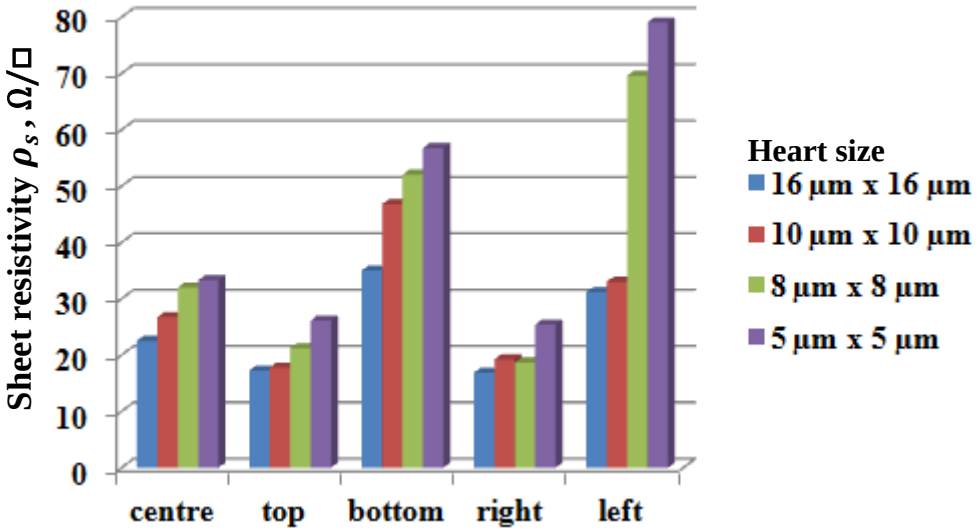


Figure 5.12 *The sheet resistivity measurement at the positions close to the centre, top, bottom, right and left section of the wafer with respect to different heart size of the Greek cross structures. The decrease in heart size increases the resistivity.*

5.5.3 Measurement and optimisation of contact resistivity for source/drain

In our study, aluminium 1 % silicon has been used as the metalisation layer and the metal comes into contact with the phosphorus implanted source/drain regions. All metal-semiconductor contacts exhibit the interfacial contact resistance R_c and becomes one of the intrinsic parasitic resistances that limit the performance of MOSFET devices [94][98][102]. Similar with the design of sheet resistivity for the source/drain regions, the interfacial contact resistance value is desired to be reasonably small in order for the *n*-MOSFET devices to gain good drain current conductions. The main concern would be to make sure that there is sufficient current flow with low voltage drop across the interfacial contact.

The typical values of the specific interfacial contact resistivity ρ_c for source/drain of the MOSFET devices have been measured and simulated to be in $\rho_c \sim 10^{-6} - 10^{-8}\ \Omega cm^2$ range [97]-[100]. As the MOSFET scales down to smaller regime, the interfacial contact resistance for source/drain of contact area $1\ \mu m \times 1\ \mu m$ has been measured to be $R_c = 30\ \Omega$ [102]. In this section, Kelvin resistor test structures have been fabricated in order to investigate the interfacial contact resistance between the aluminium 1 % silicon layer and the phosphorus implanted source/drain regions of dose $= 1e^{16}\ ions/cm^2$ and energy $= 40\ keV$. The influence of contact area on the interfacial contact resistance has been studied. For our *n*-MOSFET devices, $R_c < 30\ \Omega$ is targeted and the design of contact area has been optimised in order to achieve this.

5.5.3.1 Fabrication of Kelvin resistor test structure

Kelvin resistor test structure is a 4-point probing technique that measures the interfacial contact resistance between two conductive layers. In order to characterise the interfacial contact resistance of the source/drain terminals in our *n*-MOSFET devices, aluminium 1% silicon layer and phosphorus implanted regions have been employed in the Kelvin resistor test structure. The geometrical dimensions of the Kelvin resistor structure are illustrated in Figure 5.13 and its fabrication steps are similar with the Greek cross test structure's described previously in Figure 5.9.

Four sizes of interfacial contact area, $a \times b$ have been considered for the Kelvin resistor structure which are $5\ \mu m \times 5\ \mu m$, $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$. The electrical characteristics of the interfacial contacts have been probed electrically. The voltage across pad F and G is measured when the drive current is forced between pad E and H, giving the interfacial contact resistances of $R_1 = \frac{V_{FG}}{I_{EH}}$ and $R_2 = \frac{V_{GF}}{I_{HE}}$. The measurement is repeated by exchanging the voltage and current pads giving $R_3 = \frac{V_{EH}}{I_{FG}}$ and $R_4 = \frac{V_{HE}}{I_{GF}}$. The average of these measured four resistances will give the total interfacial contact resistance of R_c between the implanted phosphorus regions and the aluminium 1% silicon metal. The specific

interfacial contact resistivity can then be derived as $\rho_c = R_c A_k$ where A_k is the area of the interfacial contact, $a \times b$ [94][95].

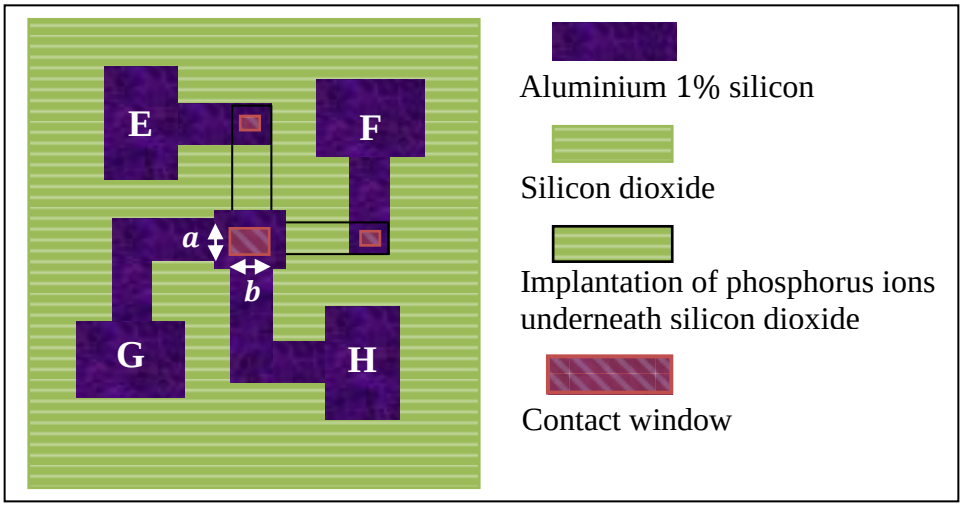


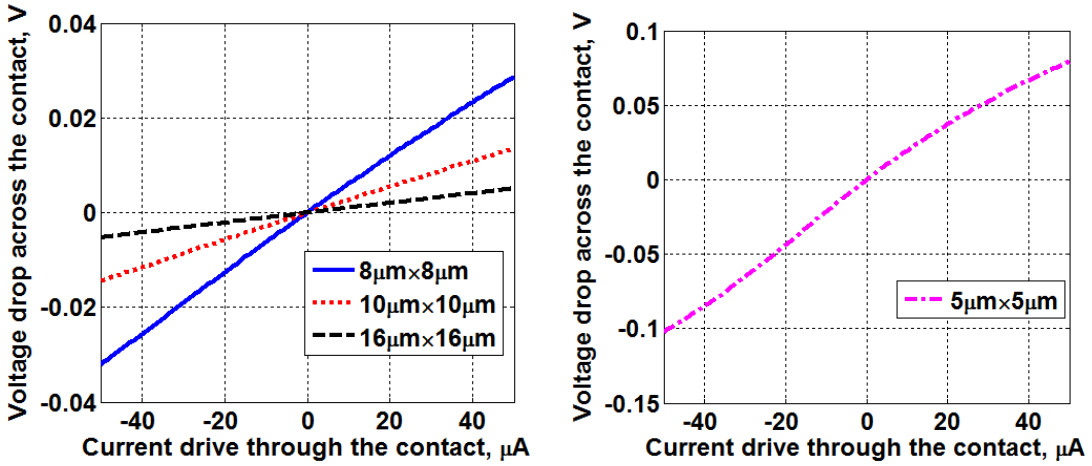
Figure 5.13 *The geometrical dimensions of the Kelvin resistor test structure. $a \times b$ defines the interfacial contact area.*

5.5.3.2 Measurement of Kelvin resistor test structure

The measured current-voltage curves of the interfacial contact between aluminium 1 % silicon layer and the phosphorus implanted region at four different contact areas are shown in Figure 5.14. Linear current-voltage curves have been achieved for $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$ while non-linear current-voltage characteristic has been measured for the contact area of $5\ \mu m \times 5\ \mu m$. This signifies that better ohmic contacts have been obtained for the larger contact areas. In addition, the increase in gradient as the contact area decreases indicates that higher interfacial contact resistance R_c has been developed as the interfacial contact area becomes smaller.

The interfacial contact resistances R_c have been measured from the gradient of the linear current-voltage characteristics with the contact areas of $8\ \mu m \times 8\ \mu m$, $10\ \mu m \times 10\ \mu m$ and $16\ \mu m \times 16\ \mu m$. Then, the specific interfacial contact resistivities ρ_c have been derived. In Figure 5.15, the measured ρ_c at five different positions on the wafer have been plotted and the values have been observed to vary across the wafer. The variation in sheet resistivity due to the non-uniform

distribution profile of the boron-doped substrate has been postulated to cause the variation in the interfacial contact resistivities across the wafer [101].



(a) Linear characteristics **(b)** Non-linear characteristics

Figure 5.14 *The measured current-voltage characteristics of the interfacial contact between aluminium* 1% *silicon and phosphorus implantation region of dose* $1e^{16}$ $ions/cm^2$ *and energy* 40 keV. *The decrease in interfacial contact area has increased the gradient i.e. the interfacial contact resistance* R_c.

The variation of ρ_c with respect to the size of the interfacial contact area in Figure 5.15 indicates that the contacts between aluminium 1 % silicon layer and the implanted phosphorus regions are non-uniform and imperfect [103]. Practically, the real contact of metal-semiconductor is not that smooth and intimate [94].

5.5.3.3 Optimisation of the interfacial contact

From Figure 5.15, the measured specific interfacial contact resistivities for the source/drain of *n*-MOSFET are within $\rho_c \sim 10^{-5} - 10^{-4}\ \Omega cm^2$ range which is relatively higher compared to the ones published in the literatures. Contact misalignment and insufficient phosphorus surface concentration in the source/drain can lead to higher measurement of ρ_c [99][100]. An epitaxial silicon layer might have as well regrown from the aluminium 1 % silicon metal. The presence of this epitaxial silicon layer between the original silicon surface and the aluminium 1 %

silicon metal layer can increase the contact resistance [94]. Other parasitic interfacial layer that can exist is the native oxide, probably due to poor substrate cleaning or poor vacuum used during the metal deposition process [94].

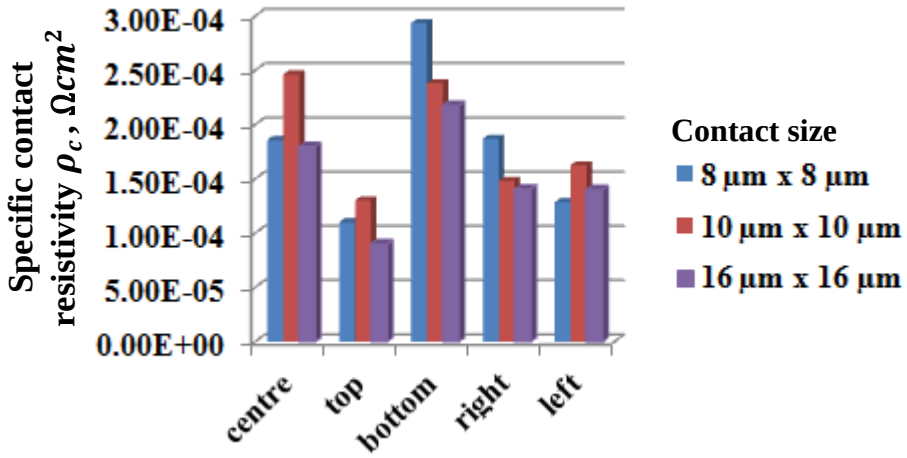


Figure 5.15 *The specific interfacial contact resistivity measurement at the positions close to the centre, top, bottom, right and left section of the wafer with respect to the different interfacial contact area of the Kelvin resistor test structures. The variation of ρ_c for different interfacial contact area signifies that the contacts are non-uniform.*

In Figure 5.14, the interfacial contact resistance R_c has been measured to decrease as the interfacial contact area increases. In addition, $R_c < 30\ \Omega$ is desired for our *n*-MOSFET devices. Therefore, the interfacial contact area for our source/drain regions will be increased in order to minimise the interfacial contact resistance [99]. The maximum interfacial contact resistivity of $\rho_c \sim 10^{-4}\ \Omega cm^2$ has been measured between the aluminium 1 % silicon layer and the phosphorus implanted source/drain regions of dose $= 1e^{16}\ ions/cm^2$ and energy $= 40\ keV$. From $\rho_c \sim 10^{-4}\ \Omega cm^2$, a reasonable interfacial contact resistance of $R_c = 3\ \Omega$ can be achieved by designing the interfacial contact area for source/drain regions to be $80\ \mu m \times 40\ \mu m$. These dimensions will be employed for the source/drain regions of the *n*-MOSFET devices which have been fabricated and measured in Chapter 6.

5.6 Conclusion

The *n*-MOSFET has been developed in order to characterise the electrical part of *n*-RGT. Thus, the fabrication process and fabrication design of the enhancement and depletion mode *n*-MOSFET have been studied in this chapter. The fabrication process for *n*-MOSFET requires the formation of 1) channel region by ion implantation technique and gate oxidation process and 2) source/drain regions by ion implantation technique and metal-semiconductor interfacial contact development. Therefore, the designs for *n*-MOSFET are focused on the 1) threshold voltage of the channel, 2) sheet resistivity of source/drain and 3) interfacial contact resistivity of source/drain. Good drain current conduction can be achieved from *n*-MOSFET with the design of small interfacial contact and sheet resistivities for the source/drain regions. The designed channel and source/drain regions in this chapter will be used to fabricate the *n*-MOSFET and *n*-RGT devices in Chapter 6.

For enhancement mode channel, the threshold voltage has been simulated to become negative in the presence of the built-in positive oxide charges within the gate oxide, Q_{ss}. The negative threshold voltage of $V_{th} = -1.1\,V$ has been expected from the enhancement mode channel with the presence of $Q_{ss} = q(3e^{11})cm^{-2}$ and the designed gate oxide thickness of t_{ox}~$70\,nm$. The measured threshold voltage of V_{th}~$-1.2\,V$ from the fabricated enhancement mode *n*-MOSFETs in Chapter 6 verified the presence of Q_{ss}.

For depletion mode channel, the phosphorus ions implantation technique has been used to create the channel. The phosphorus surface concentration has been simulated to be the control parameter that determines the threshold voltage of the depletion mode *n*-MOSFET. Assuming $Q_{ss} = q(3e^{11})cm^{-2}$, the phosphorus ion doses of $8e^{11}\ ions/cm^2 - 2e^{12}\ ions/cm^2$, energy of $40\,keV$ and t_{ox}~$70\,nm$ have been designed in order to obtain the phosphorus surface concentrations of $3e^{15}\ atoms/cm^3 - 7e^{15}\ atoms/cm^3$ and threshold voltage within $-3\,V$ to $-1\,V$. The phosphorus surface concentrations of the depletion mode channel have been measured using the SIMS technique and have been found to be consistent with the

simulation. Using the designed parameters, the depletion mode *n*-MOSFETs have been fabricated in Chapter 6 with V_{th} within $-3\ V$ to $-1\ V$.

The phosphorus ions implantation technique has also been employed in order to form the source/drain regions. The dose and energy for the implantation of the source/drain regions have been designed to be $1e^{16}\ ions/cm^2$ and $40\ keV$, respectively in order to obtain small sheet resistivity of $20.4\ \Omega/\square$. The average sheet resistivity of the phosphorus implanted source/drain regions has been extracted using the Greek cross test structure to be $\rho_s = 25.93\ \Omega/\square$, higher than the designed value probably due to the heating effect within the structure.

Finally, the design of the interfacial contact for the source/drain regions has been carried out using the Kelvin resistor test structure. Aluminium 1 % silicon has been employed as the metal electrode that comes in contact with the phosphorus implanted source/drain regions through the pre-defined contact windows. As the interfacial contact area increases, better ohmic contact with linear current-voltage characteristics has been obtained. Furthermore, the interfacial contact resistance R_c has been measured to decrease with the increase of the interfacial contact area. The maximum specific interfacial contact resistivity of $\rho_c{\sim}10^{-4}\ \Omega cm^2$ has been extracted between the aluminium 1 % silicon layer and the phosphorus implanted source/drain regions of dose $1e^{16}\ ions/cm^2$ and energy $40\ keV$. From $\rho_c{\sim}10^{-4}\ \Omega cm^2$, the interfacial contact area for the source/drain regions have been designed to be approximately $80\ \mu m \times 40\ \mu m$ in order to achieve the reasonable interfacial contact resistance of $R_c = 3\ \Omega$.

Chapter 6: The measurement and characterisation of *n*-MOSFET and *n*-RGT

6.1 Introduction

In Chapter 5, the fabrication process and design of the *n*-type channel and source/drain regions for the *n*-channel metal-oxide-semiconductor field-effect transistor (*n*-MOSFET) have been described. In this chapter, the enhancement and depletion mode *n*-MOSFETs will be fabricated and DC measurement will be performed on the devices. The chapter starts with the measurement and characterisation of the threshold voltage, transconductance and subthreshold current for the enhancement mode *n*-MOSFETs. Then, the investigation continues with the measurement and characterisation for the depletion mode *n*-MOSFETs. The effect of channel width to channel length ratio on the transconductance will be studied.

The fabricated *n*-type channel and source/drain regions will be integrated with the bridge gate structure to create the *n*-channel resonant gate transistor (*n*-RGT). The integration of the aluminium bridge gate and tantalum bridge gate with the *n*-type channel will be known as the *n*-channel resonant aluminium gate transistor (*n*-RAGT) and *n*-channel resonant tantalum gate transistor (*n*-RTGT), respectively. The operating range of the DC current and voltage for the *n*-RGT devices will be measured. The pull-in voltage and electromechanical behaviour of the *n*-RGT devices will be investigated. Basically, the operating bridge gate voltage for the *n*-RGT should lie between the pull-in voltage of the bridge gate and the threshold voltage of the *n*-type channel. The measurement and characterisation of the

threshold voltage, transconductance and subthreshold current for the *n*-RAGT and *n*-RTGT will be performed and compared with those measured from the *n*-MOSFETs. The effects of introducing the air gap spacing between the bridge gate and the *n*-type channel region on the threshold voltage and transconductance of the *n*-RGT device will be discussed.

6.2 Summary of *n*-MOSFET and *n*-RGT design

The fabrication processes to create the *n*-type channel and source/drain have been discussed in Chapter 5. The schematic diagram for the channel region and source/drain of the *n*-MOSFET and *n*-RGT are depicted in Figure 6.1. The length and width of the channel region are labelled as L_c and W_c while the length of the phosphorus implanted source/drain regions is indicated by SD_L. The interfacial contact area between the phosphorus implanted source/drain regions and the aluminium 1 % silicon electrode layer is defined by $SD_L \times W_c$.

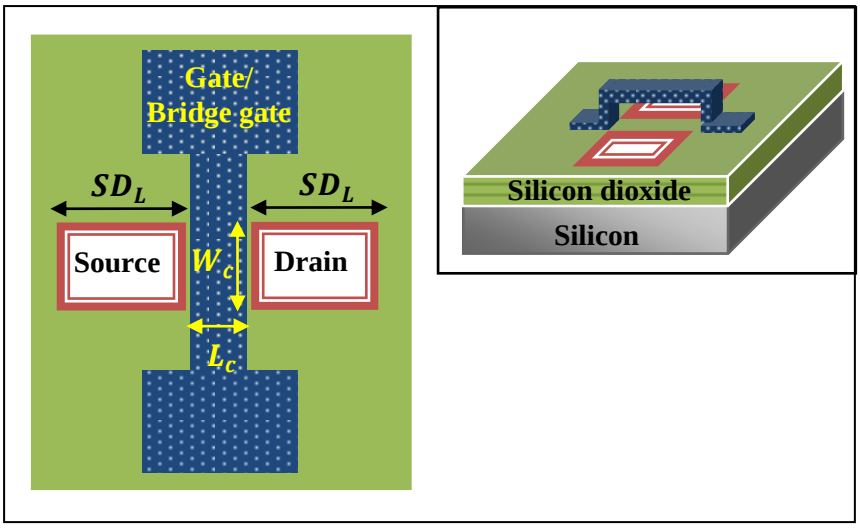


Figure 6.1 *Top view of the n-MOSFET(n-RGT) showing the gate(bridge gate), channel of size $W_c \times L_c$ and source/drain regions of size $SD_L \times W_c$. Subset shows the 3-dimensional view of the n-RGT.*

The geometrical dimensions used for the *n*-channel devices are summarised in Table 6.1. In the first iteration, the size of channel length is varied between $L_c = 5\ \mu m - 10\ \mu m$ while the size of channel width is varied between $W_c = 25\ \mu m - 540\ \mu m$,

giving the channel width to length ratios of $\frac{W_c}{L_c} = 2.5 - 108$. For $SD_L = 40\ \mu m$, the interfacial contact area at source/drain is given by $40\ \mu m \times W_c$. From the measured maximum specific interfacial contact resistivity of $\rho_c \sim 10^{-4}\ \Omega cm^2$ in Chapter 5, the reasonable interfacial contact resistances of $R_c = 0.4 - 10\ \Omega$ can be achieved for the source/drain. In this iteration, the enhancement mode *n*-MOSFETs have been fabricated and the wafer is labelled as $W10$. For the fabrication of depletion mode *n*-MOSFETs, the wafers are labelled as $W2$ and $W8$ with the phosphorus ions beam dose of $8e^{11}\ ions/cm^2$ and $2e^{12}\ ions/cm^2$ applied on the channel. The wafers have been annealed at 1100 ℃ for 30 $minutes$ and the gate oxide has been grown thermally at 1100 ℃ for 30 $minutes$. The gate oxide thickness for the fabricated *n*-channel devices have been measured to be $t_{ox} = 70 \pm 5\ nm$. The fabrication steps to create the enhancement and depletion mode *n*-MOSFET can be referred in Figure 5.2 and Figure 5.3, respectively.

No	Device	Type	Label	L_c (μm)	W_c (μm)	SD_L (μm)	t_{ox} (nm)	d_i (μm)
1	*n*-MOSFET	EM	$W10$	$5 - 10$	$25 - 540$	40	70	-
	n-MOSFET	DM	$W8$	$5 - 10$	$25 - 540$	40	70	-
	n-MOSFET	DM	$W2$	$5 - 10$	$25 - 540$	40	70	-
2	*n*-MOSFET	EM	WE	$10 - 20$	$40 - 80$	40	77	-
	n-RAGT	EM	WE	$10 - 20$	$40 - 80$	40	77	4
3	*n*-MOSFET	EM	WF	$10 - 20$	$40 - 80$	40	55	-
	n-RTGT	EM	WF	$10 - 20$	$40 - 140$	40	55	7-13

Table 6.1 *Summary of the geometrical dimensions used for the fabrication and characterisation of the n-MOSFET and n-RGT. EM: Enhancement mode DM: Depletion mode.*

In the second and third iterations, the range of channel length has been increased to $L_c = 10\ \mu m - 20\ \mu m$ while the channel width range of $W_c = 40\ \mu m - 140\ \mu m$ has been considered. In addition, the temperatures used for the annealing step of the

implantation regions and for the gate oxidation process have been reduced. The changes made in the dimensions of the device and the optimisations of the temperature used in fabrication have been suggested in order to resolve the channel breakdown issue within the devices.

In the second iteration, the enhancement mode *n*-MOSFETs have been fabricated and the wafer is labelled as WE. The furnace temperature used to anneal the implantation regions has been reduced to 1000 ℃ for 30 $minutes$ and the gate oxide has been grown thermally at 1100 ℃ for 30 $minutes$. The gate oxide of the fabricated devices in the second iteration has been measured to be $t_{ox} = 77 \pm 2\ nm$. For the second iteration, the aluminium bridge gate structure has been integrated with the enhancement mode *n*-type channel to become the enhancement mode *n*-channel resonant aluminium gate transistor (*n*-RAGT). The distance from the aluminium bridge gate to the channel region has been measured to be $d_i \sim 4\ \mu m$.

In the third iteration, the enhancement mode *n*-MOSFETs have been fabricated and the wafer is labelled as WF. The temperature for annealing has been further reduced to 950 ℃ for 30 $minutes$ and the gate oxide has been grown thermally at 950 ℃ for 30 $minutes$. The gate oxide of the fabricated devices from the third iteration have been measured to be $t_{ox} = 55 \pm 2\ nm$. For wafer WF, the tantalum bridge gate has been integrated with the enhancement mode *n*-type channel to become the enhancement mode *n*-channel resonant tantalum gate transistor (*n*-RTGT). The distance from the tantalum bridge gate to the channel region has been measured to be $d_i \sim 7\ \mu m - 13\ \mu m$.

6.3 DC measurement of *n*-MOSFET

The fabricated *n*-MOSFETs have been measured using Hewlett Packard 4156B Semiconductor Parameter Analyzer in order to obtain the electrical output characteristics of the devices. The curves of drain current against drain voltage (i.e. $I_{ds} - V_{ds}$ characteristics) of the four-terminal *n*-MOSFET device are obtained by varying the drain voltage V_{ds} and gate voltage V_{gs}, with the source and substrate

being grounded and the drain current I_{ds} being measured. The *n*-MOSFETs have been observed to operate within the linear and saturation regimes.

A family of transconductance curves (i.e. $g_m - V_{gs}$ characteristics) in the linear regime has been plotted and used to extract the threshold voltage V_{th} of the fabricated *n*-MOSFET. The threshold voltage has been determined from the extrapolation of the transconductance curves at small values of drain voltages in order to ensure that the device operation is within the linear regime [87][88].

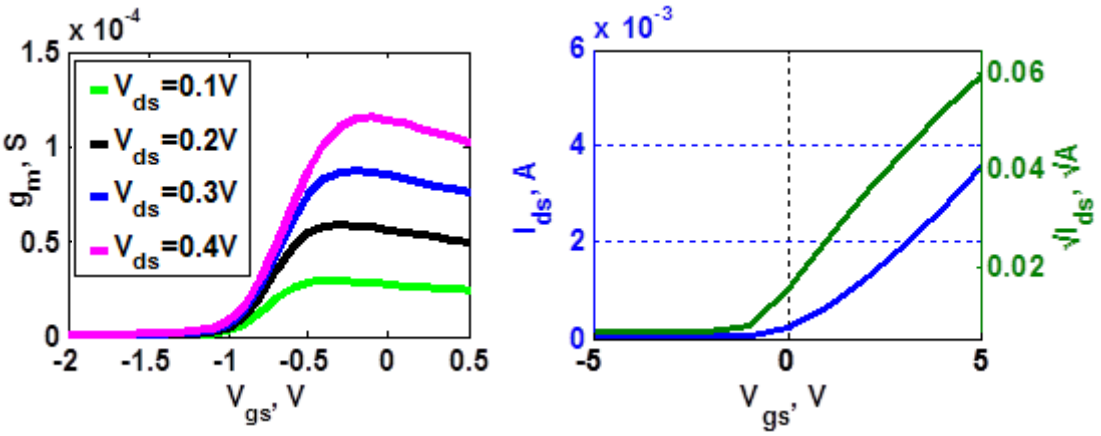
Meanwhile, the transfer characteristics (i.e. $I_{ds} - V_{gs}$ characteristics) in the saturation regime has been plotted and used to measure the transconductance of the fabricated *n*-MOSFET. The maximum transconductance g_m has been extracted from the gradient of the transfer characteristics at a certain value of gate voltage [109][110]. From the transfer characteristics in the saturation regime, the threshold voltage can also be extracted by plotting the $\sqrt{I_{ds}} - V_{gs}$ characteristics and compared with the one measured from the linear regime [94].

6.3.1 The first iteration: Enhancement and depletion mode *n*-MOSFET

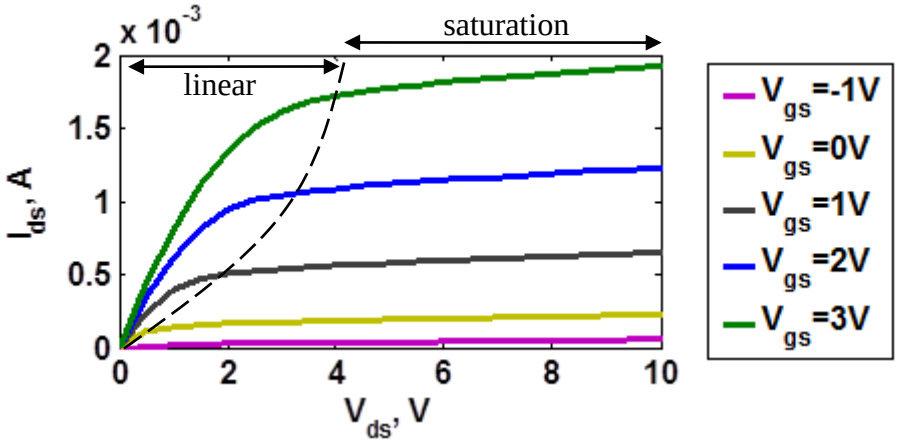
The enhancement mode *n*-MOSFETs have been fabricated on a 3-inch *p*-type boron-doped silicon wafer labelled as $W10$ with the nominal bulk resistivity of $\rho = 14\ \Omega cm - 20\ \Omega cm$. The DC measurement results for the enhancement mode *n*-MOSFETs with t_{ox}~$70\ nm$, $L_c = 10\ \mu m$ and $W_c = 80\ \mu m$ are shown in Figure 6.2. Reasonably accurate estimation of V_{th} in the linear regime can be obtained by plotting the $g_m - V_{gs}$ characteristics at small values of V_{ds} [Figure 6.2(a)]. The linear portions of the curves are extrapolated to the V_{gs} axis. The voltage at the interception can be equated as the threshold voltage [87][88]. The threshold voltage for the enhancement mode *n*-MOSFET has been extracted from the linear regime to be approximately $V_{th} = -1\ V$.

From the transfer characteristics ($I_{ds} - V_{gs}$) of the enhancement mode *n*-MOSFET working in the saturation regime [Figure 6.2(b)], a subthreshold current of $I_{th} =$

58 μA has been measured at $V_{th} = -1\ V$. The maximum transconductance from the maximum gradient of the transfer characteristics has been extracted to be $g_m = 1\ mS$ at $V_{gs} = V_{th} + 3\ V$ and $V_{ds} = 10\ V$.



(a) Transconductance curves **(b)** $\sqrt{I_{ds}} - V_{gs}$ and transfer characteristics



(c) $I_{ds} - V_{ds}$ characteristics

Figure 6.2 *The DC measurements of the enhancement mode n-MOSFET with $L_c = 10\ \mu m$, $W_c = 80\ \mu m$ and t_{ox}~70 nm from wafer W10. (a) $g_m - V_{gs}$ characteristics in the linear regime extract $V_{th} = -1\ V$. (b) The $\sqrt{I_{ds}} - V_{gs}$ characteristics and the transfer characteristics in the saturation regime at $V_{ds} = 10\ V$ measure $V_{th} = -1\ V$ and $g_m = 1\ mS$. (c) The $I_{ds} - V_{ds}$ characteristics showing the linear and saturation regimes.*

The threshold voltage can also be extracted from the saturation regime by plotting and extrapolating the $\sqrt{I_{ds}} - V_{gs}$ curves in Figure 6.2(b) to zero drain current. From

the interception at V_{gs} axis, the threshold voltage of approximately $V_{th} = -1\,V$ has been determined from the saturation regime. The measured threshold voltage from the linear and saturation regimes agree well with the simulated value of $V_{th} = -1.1\,V$ from section 5.4.1 in Chapter 5, assuming $Q_{ss} = q(3e^{11})cm^{-2}$ with $q = 1.6e^{-19}\,C$. The presence of positive oxide charges Q_{ss} within the gate oxide has been simulated previously to cause the threshold voltage for the enhancement mode *n*-MOSFET to become negative.

6.3.1.1 Depletion mode characteristics and negative threshold voltage due to *Qss*

The $I_{ds} - V_{ds}$ characteristics of the enhancement mode *n*-MOSFET for $V_{ds} = 0\,V - 10\,V$ is shown in Figure 6.2(c). The device has been observed to enter the saturation regime when $V_{ds} = V_{gs} - V_{th}$ with the drain current in the saturation regime increases from I_{ds}~0 μA to 1.9 mA for the increase of gate voltage from $V_{gs} = -1\,V$ to $3\,V$. The device operates as a depletion mode instead of enhancement mode in which there is significant drain current flow at $V_{gs} = 0\,V$. The device is normally on and requires $V_{gs} < V_{th}$ to be turned off. The current decreases (increases) as V_{gs} becomes more negative (positive).

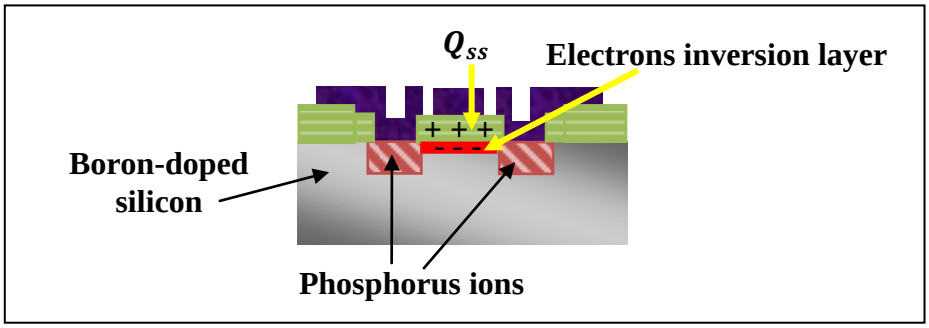


Figure 6.3 *The presence of positive oxide charges Q_{ss} at the gate oxide-silicon channel interface of the enhancement mode n-MOSFET at $V_{gs} = 0\,V$. Q_{ss} induces the formation of electrons inversion layer, causing the conduction of drain current at $V_{gs} = 0\,V$.*

Due to the light doping of boron substrate, the fabricated *n*-MOSFETs on the boron-doped silicon substrate have been reported to possess the built-in electrons inversion

layer in the absence of any applied gate voltage [Figure 6.3] [87]. Thus, the electrons inversion layer exists at $V_{gs} = 0\ V$ and enhanced when V_{gs} is made positive or depleted when V_{gs} is made negative. The trapped positive ion species within the gate oxide i.e. the positive oxide charges Q_{ss}, located close to the gate oxide-silicon channel interface has been suspected to induce the formation of electrons inversion layer within the lightly boron-doped substrate, resulting in the depletion mode characteristics and negative threshold voltage for the enhancement mode *n*-MOSFET.

6.3.1.2 Channel length modulation

In saturation, the drain current for each V_{gs} has been observed to increase as a function of V_{ds}, indicating the presence of channel length modulation within the fabricated device. Channel length modulation is caused by the increase in the depletion layer width of the drain as the applied V_{ds} increases, making the channel length shorter and thus larger flows of drain current during the operation [104]. For $V_{gs} = 0\ V$ in Figure 6.2(c), the output saturation drain current increases at the rate of $\sim 36.2\ \mu A/V$ with respect to the increase of V_{ds}. The corresponding drain-source shunt resistance has been measured as $r_{ds} \sim 27.6\ k\Omega$. Thus, the channel length modulation parameter, λ that quantifies the influence of V_{ds} on the saturation drain current has been estimated to be $\lambda = 1/r_{ds} I_{ds(sat)} \sim 0.18\ V^{-1}$.

6.3.1.3 Influence of W_c/L_c ratio on transconductance

From wafer $W10$, the channel width has been increased from $W_c = 25\ \mu m$ to $540\ \mu m$. Therefore, the channel width to channel length ratio increases from $\frac{W_c}{L_c} = 2.5$ to 54 for the enhancement mode *n*-MOSFETs of channel length $L_c = 10\ \mu m$. The transconductance, threshold voltage and subthreshold current have been measured and tabulated with respect to $\frac{W_c}{L_c}$ ratio in Table 6.2. As the ratio increases, the transconductance g_m increases from $0.38\ mS$ to $4.46\ mS$. This is consistent with the theoretical prediction that higher transconductance values can be achieved

by employing higher $\frac{W_c}{L_c}$ ratios [87]. The design of $\frac{W_c}{L_c}$ ratio from 8 to 54 for the channel region of the enhancement mode *n*-MOSFETs in Table 6.2 gives reasonably high transconductance values of $g_m = 1.0\ mS - 4.46\ mS$. Thus, strong modulations of the channel conductance induced by the gates have been obtained from the corresponding devices.

W_c/L_c	2.5	8	12.5	26	40	54
$g_m\ (mS)$	0.38	1.00	1.58	2.49	3.27	4.46
$V_{th}\ (V)$	−2	−1	−1	−1	−1	−1
$I_{th}\ (mA)$	0.11	0.06	0.40	0.11	0.80	0.99

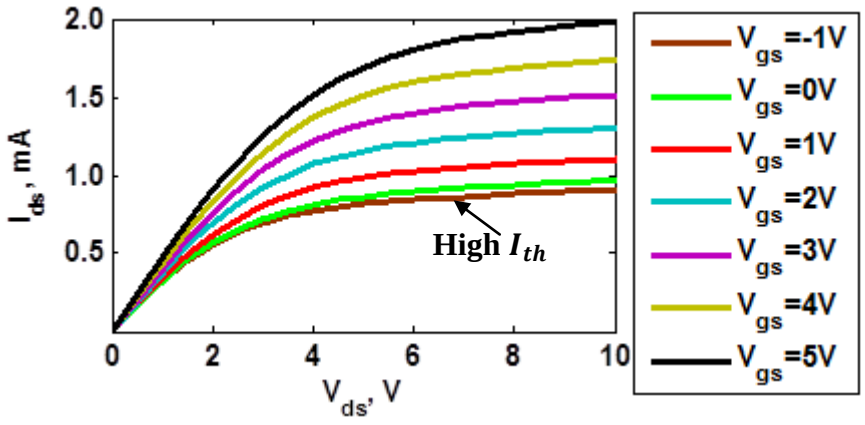
Table 6.2 *The measured transconductance, threshold voltage and subthreshold current from the enhancement mode n-MOSFETs of channel length $L_c = 10\ \mu m$ and a variation of channel width from $W_c = 25\ \mu m$ to $540\ \mu m$ in wafer $W10$. The measured transconductance increases with respect to the increase in $\frac{W_c}{L_c}$ ratio.*

6.3.1.4 High subthreshold leakage current

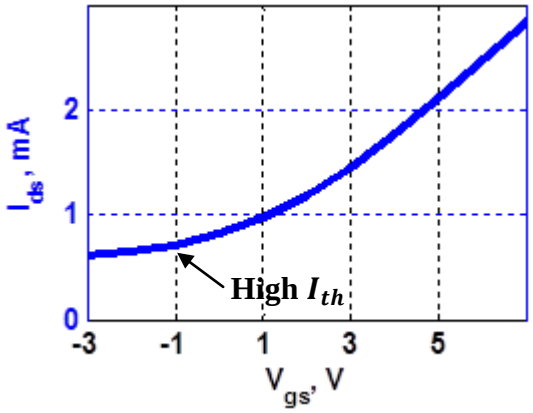
In Table 6.2, an average threshold voltage of $-1.2\ V$ has been measured from the enhancement mode *n*-MOSFETs which have been fabricated on the same chip from wafer $W10$. At $V_{th} = -1.2\ V$, the measured subthreshold currents have been observed to be inconsistent and can become relatively high, close to $1\ mA$ in some devices. An example of the high subthreshold current measurement from the enhancement mode *n*-MOSFET with $V_{th} = -1.2\ V$ is shown in Figure 6.4.

The device has been observed to be turned off with high subthreshold leakage current flowing between source and drain, leading to high energy consumption. In section 5.5.2.2, the concentration of boron doping within the substrate has been postulated to be non-uniform across the wafer. The measured high subthreshold leakage current on some devices might be related to the sudden decrease in boron substrate doping

and thus, stronger electrons inversion layer has been induced by Q_{ss} in the channel of the enhancement mode *n*-MOSFET.



(c) $I_{ds} - V_{ds}$ characteristics



(b) Transfer characteristics

Figure 6.4 *High subthreshold leakage current I_{th} has been measured from the (a) $I_{ds} - V_{ds}$ characteristics and (b) transfer characteristics of the enhancement mode n-MOSFET device.*

Further increase in the negative V_{gs} applied onto the gate was unable to deplete the electrons inversion layer and thus reduces the transconductance. Transconductance is a parameter that quantifies the strength in modulation of the channel conductance. High subthreshold current problem has been observed to reduce the strength in modulation of the channel conductance with respect to the applied gate voltage. Therefore, it is crucial to minimise this leakage current in order to maintain high transconductance value for the device. In the next section, the depletion mode *n*-MOSFETs have been fabricated in wafer $W8$ and $W2$. The high subthreshold

leakage current problem has been found to be severe within the depletion mode devices.

6.3.1.5 Influence of W_c/L_c ratio on channel breakdown in depletion mode *n*-MOSFET

The depletion mode *n*-MOSFETs have been fabricated on a 3-inch *p*-type boron-doped silicon wafer with the nominal bulk resistivity of $\rho = 14\ \Omega cm - 20\ \Omega cm$. The depletion mode channel has been implanted using the phosphorus ions beam with energy of 40 keV and doses of $2e^{12}\ ions/cm^2$ (wafer $W8$) and $8e^{11}\ ions/cm^2$ (wafer $W2$). In Table 6.3, the average threshold voltage for the fabricated depletion mode *n*-MOSFETs in wafer $W8$ with $\frac{W_c}{L_c}$ ratio of 2.5 and 8 has been measured to be $V_{th} = -3\ V$. The measured negative threshold voltage is slightly higher than the simulated $V_{th} = -2.54\ V$ in section 5.4.2.1 in Chapter 5, for the implantation dose of $2e^{12}\ ions/cm^2$ and assuming $Q_{ss} = q(3e^{11})cm^{-2}$.

W_c/L_c	2.5	8	12.5	26	40	54
$g_m\ (mS)$	0.46	1.06	CB	CB	CB	CB
$V_{th}\ (V)$	-3	-3	CB	CB	CB	CB
$I_{th}\ (mA)$	2.15	4.85	CB	CB	CB	CB

Table 6.3 *The measured transconductance, threshold voltage and subthreshold current from the depletion mode n-MOSFETs of channel length $L_c = 10\ \mu m$ and a variation of channel width from $W_c = 25\ \mu m$ to $540\ \mu m$ in wafer $W8$. CB indicates channel breakdown. The increase in $\frac{W_c}{L_c}$ ratio promotes channel breakdown within the device.*

As the $\frac{W_c}{L_c}$ ratio increases from 2.5 to 8, the measured transconductance increases in a similar pattern with those measured from the enhancement mode devices in wafer $W10$. However, the measured subthreshold currents have been observed to be

$I_{th} > 1\ mA$ and many times higher than $W10$. For the depletion mode *n*-MOSFETs of $\frac{W_c}{L_c} > 8$, channel breakdown have been observed. The gate loses control over the channel and the drain current has been measured to be very dependent on V_{ds}.

Similar high subthreshold currents of $I_{th} > 1\ mA$ have been observed for the fabricated depletion mode *n*-MOSFETs from wafer $W2$. The average threshold voltage from $W2$ with $\frac{W_c}{L_c} < 8$ has been measured to be $V_{th} = -2\ V$ which is slightly higher than the simulated $V_{th} = -1.58\ V$ for the implantation dose of $8e^{11}\ ions/cm^2$. Channel breakdown has been measured for the depletion mode *n*-MOSFETs from wafer $W2$ with $\frac{W_c}{L_c} > 8$. Overall, the increase in $\frac{W_c}{L_c}$ ratio promotes channel breakdown within the device.

6.3.1.6 Channel breakdown in enhancement and depletion mode *n*-MOSFETs for L_c< 10 μm

The enhancement and depletion mode *n*-MOSFETs of channel length $L_c < 10\ \mu m$ have been fabricated and studied. For the enhancement mode *n*-MOSFETs, the subthreshold currents of higher than $1\ mA$ have been measured and 40 % of the fabricated devices suffer from the channel breakdown. As for the depletion mode, the number of devices with channel breakdown is almost 90%.

The decrease in L_c increases $\frac{W_c}{L_c}$ ratio which means that the possibility of the devices experiencing channel breakdown will be higher. In this regime, the increase of $\frac{W_c}{L_c}$ ratio has been found to 1) increase the subthreshold current for the enhancement mode device to be more than $1\ mA$ and 2) increase the number of channel breakdown for both type of devices.

6.3.1.7 Source of channel breakdown and high subthreshold leakage current

In drain current conduction, the number of charge carriers within the electrons inversion layer is controlled by the gate voltage [104]. In real MOSFET, the leakage

currents at the drain-substrate junction and across the depletion region underneath the channel contribute to the measured drain current [104]. When the device is off, the total leakage currents are measured as the subthreshold current or also known as the off-state leakage current [106]-[108]. A considerably small subthreshold leakage current is desired in order to minimise device heating and energy consumption when the device is off.

The measured high subthreshold leakage current has been described in section 6.3.1.4 to be related to the light doping of boron substrate. The boron segregation effect might also have contributed to the decrease of boron concentration at the silicon channel surface. Therefore, stronger electrons inversion layer has been induced by Q_{ss} within the channel of the devices, leading to high subthreshold leakage current and in the worst case scenario, the channel breakdown.

The second order effect that might have caused channel breakdown and high subthreshold leakage current is the domination of the electric field from drain voltage over the electric field from gate voltage. In section 5.4.3.2 in Chapter 5, the channel length has been designed to be sufficiently long in order to prevent short channel effects. However, with the application of V_{ds}, the depletion region around drain broaden. Thus, the distance between source and drain i.e. channel length decreases. The influence of electric field from drain voltage on the channel will be greater and can dominate over the perpendicular electric field from gate voltage, causing effects similar to short channel [87][94][104]. Therefore, the increase of channel breakdown and subthreshold leakage current from both enhancement and depletion mode devices as $\frac{W_c}{L_c}$ ratio increases have been suspected to be related to the presence of high electric field within the channel exerted by the drain voltage.

The induced high electric field within the channel 1) reduces the barrier for the electrons to enter the channel and 2) generates hot electrons that possess high velocity. Hot electrons can then produce more electron-hole pairs by impact ionisation mechanism with the silicon substrate causing the high subthreshold

leakage current and channel breakdown. In addition, hot electrons can enter the gate oxide, resulting in the gate oxide charging effect that reduces the influence of gate voltage on the channel [87][94][104].

6.3.1.8 Optimisation to reduce channel breakdown and high subthreshold leakage current

The first and second order effects that cause the high subthreshold leakage current and channel breakdown problems within the *n*-channel devices can be minimised by employing thinner gate oxide, higher boron substrate doping, shallower junction depths for source/drain and longer channels [87][94][104]. In the next iterations for wafer WE and WF, the second order effects in our *n*-channel devices have been minimised by increasing the channel length from $10\ \mu m$ to $20\ \mu m$ and reducing the process temperature during the fabrication of the device.

Lower furnace temperature for the gate oxidation process and annealing of the implantation regions will help to reduce the vertical and lateral diffusions of the phosphorus implanted source/drain regions i.e. making the effective channel length to be longer and the junction depths at source/drain to be shallower. The influence of electric field from drain voltage is expected to be reduced as the drain becomes shallower and further away from the source. However, the decrease in junction depth is optimised in order to maintain small sheet resistivity for the phosphorus implanted source/drain regions. In addition, the thickness of gate oxide has been reduced to $25\ \%$ for wafer WF. The gate is closer to the channel and is expected to have more control over the electrons inversion layer [104].

6.3.2 The second iteration: Enhancement mode *n*-MOSFET

A few steps have been taken into consideration in order to resolve the high subthreshold leakage current and channel breakdown problems that occurred within the fabricated enhancement and depletion mode *n*-MOSFETs in wafer $W10$, $W8$ and $W2$. The main aim is to lessen the influence of the electric field exerted by drain voltage on the channel. In the second iteration, the channel length of $10\ \mu m -$

20 μm have been considered for the enhancement mode *n*-MOSFETs in wafer WE with the substrate resistivity of $\rho = 14\ \Omega cm - 20\ \Omega cm$. Compared to $W10$, the temperature used to anneal the implantation regions has been reduced from 1100 ℃ to 1000 ℃. The same gate oxidation parameters have been selected but the grown gate oxide layer has been measured to be t_{ox}~77 nm which is ~7 nm higher than $W10$.

$I_{th}\ (mA)$		$W_c(\mu m)$		
		40	**60**	**80**
$L_c\ (\mu m)$	**10**	1.28	2.40	7.7
	20	0.85	0.24	0.71

(a) Subthreshold current

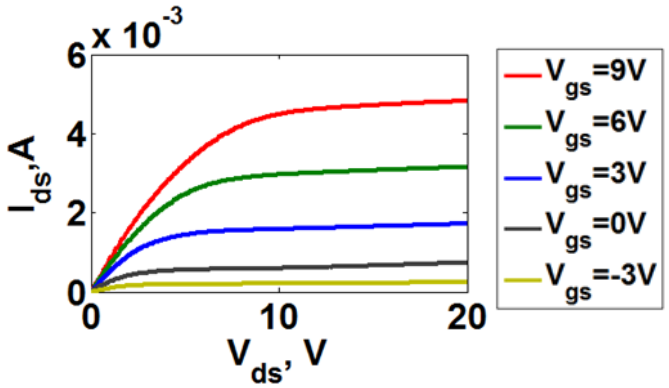
$V_{th}\ (V)$		$W_c(\mu m)$		
		40	**60**	**80**
$L_c\ (\mu m)$	**10**	−3.0	−3.5	−3.5
	20	−4.0	−3.0	−3.0

(b) Threshold voltage

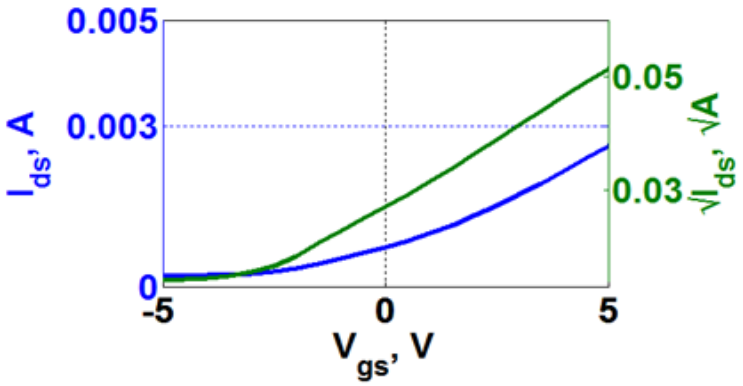
Table 6.4 *The measured (a) subthreshold current and (b) threshold voltage of the enhancement mode n-MOSFETs from wafer WE with the annealing temperature reduces to* 1000 ℃. *No channel breakdown has been observed from the fabricated devices in wafer WE.*

The measured subthreshold current and threshold voltage from the fabricated enhancement mode *n*-MOSFETs in wafer WE with respect to the different sizes of channel length and width are tabulated in Table 6.4. In wafer WE, the devices' performance have been improved compared to $W10$ with no channel breakdown being observed in the fabricated devices. The influence of electric field from the drain voltage has been minimised. However, the subthreshold current measured

from $L_c = 10\ \mu m$ is unexpectedly higher than $1\ mA$ [Table 6.4(a)]. As the channel length increases to $20\ \mu m$, the subthreshold current decreases. Overall, only 40 % of the fabricated devices from wafer WE possess the subthreshold current of less than $1\ mA$.



(a) $I_{ds} - V_{ds}$ characteristics



(b) $\sqrt{I_{ds}} - V_{gs}$ and transfer characteristics

Figure 6.5 *The DC measurements of the enhancement mode n-MOSFET with $L_c = 20\ \mu m$, $W_c = 60\ \mu m$ and t_{ox}~77 nm from wafer WE. (a) The $I_{ds} - V_{ds}$ characteristics showing the linear and saturation regimes. Channel length modulation within the device has been observed to be smaller compared to the first iteration. (b) The $\sqrt{I_{ds}} - V_{gs}$ characteristics and the transfer characteristics in the saturation regime at $V_{ds} = 20\ V$ measure $V_{th} = -3\ V$ and $g_m = 0.5\ mS$.*

Another interesting observation is that the measured threshold voltages in Table 6.4(b) are more negative than the ones measured from $W10$ even though the devices from both wafers undergo similar gate oxidation procedure. The difference in

quality and thickness of the thermally grown gate oxide layer has been suspected to affect the threshold voltage of the devices. The grown gate oxide layer for the enhancement mode *n*-MOSFETs in wafer WE is $\sim 7\,nm$ thicker with the higher estimated value of $Q_{ss} = q(8.5e^{11})\,cm^{-2}$ compared to $W10$. In addition, the surface concentration of boron-doped substrate might be different in WE which can also affect the threshold voltage.

The DC measurement results for the enhancement mode *n*-MOSFET from wafer WE with $t_{ox} \sim 77\,nm$, $L_c = 20\,\mu m$ and $W_c = 60\,\mu m$ are shown in Figure 6.5 with the measured $V_{th} = -3\,V$, $I_{th} = 0.25\,mA$ and $g_m = 0.5\,mS$. The channel length modulation parameter has been measured to be $\lambda = 1/r_{ds}I_{ds(sat)} \sim 0.04\,V^{-1}$. Overall, the channel length modulation within the fabricated enhancement mode *n*-MOSFET devices from wafer WE have been measured to be smaller compared to the first iteration from wafer $W10$.

6.3.3 The third iteration: Enhancement mode *n*-MOSFET

In the first and second iterations, the furnace temperature used for growing the gate oxide layer is 1100 ℃. In the third iteration, the temperature for gate oxidation has been reduced to 950 ℃. The thickness of the gate oxide layer has also been reduced to $55\,nm$. In addition, the temperature used to anneal the implantation regions has been further reduced from 1000 ℃ to 950 ℃. In this iteration, 80 % of the fabricated enhancement mode *n*-MOSFETs in wafer WF possess the subthreshold current of less than $1\,mA$. Therefore, the influence of electric field from drain voltage on the channel has been further reduced in this iteration by decreasing the diffusion of phosphorus implanted source/drain regions and decreasing the gate oxide thickness.

The measured subthreshold currents from the enhancement mode *n*-MOSFETs in wafer WF with respect to the different sizes of channel length and width are tabulated in Table 6.5(a). No channel breakdown has been measured from this wafer. The device performance has been improved with the minimisation of the

subthreshold current to be less than 1 mA for all channel length and channel width in Table 6.5(a). The measured threshold voltages in Table 6.5(b) show an average value of $V_{th} = -1.8\,V$ and thus, the estimated built-in positive oxide charges within 55 nm of gate oxide is approximately $Q_{ss} = q(6.9e^{11})\ cm^{-2}$.

$I_{th}\ (mA)$		$W_c(\mu m)$		
		40	**60**	**80**
$L_c\ (\mu m)$	**10**	0.05	0.03	0.01
	20	0.05	0.01	0.08

(a) Subthreshold current

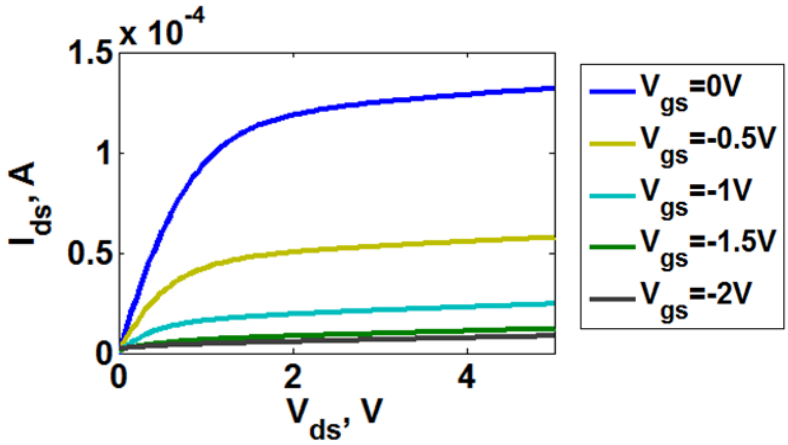
$V_{th}\ (V)$		$W_c(\mu m)$		
		40	**60**	**80**
$L_c\ (\mu m)$	**10**	-3	-1.5	-1.5
	20	-1.8	-1.5	-2

(b) Threshold voltage

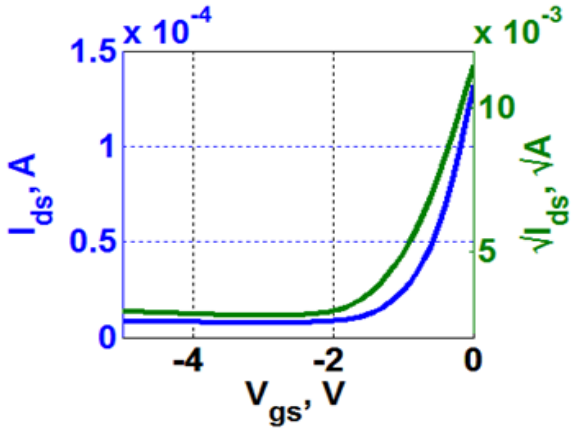
Table 6.5 *The measured (a) subthreshold current and (b) threshold voltage of the enhancement mode n-MOSFETs from wafer WF with the annealing and gate oxidation temperature reduces to* 950 ℃. *No channel breakdown has been observed from the fabricated devices in wafer WF.*

The DC measurement results for the enhancement mode *n*-MOSFET which has been fabricated in wafer WF with $t_{ox} = 55\ nm$, $L_c = 20\ \mu m$ and $W_c = 60\ \mu m$ are shown Figure 6.6 with the measured $V_{th} = -1.5\,V$, $I_{th} = 0.01\,mA$ and $g_m = 0.16\,mS$. The channel length modulation parameter has been measured to be $\lambda = 1/r_{ds}I_{ds(sat)} \sim 0.03\,V^{-1}$. The channel length modulation within the fabricated enhancement mode *n*-MOSFETs in wafer WF have been measured to be smaller compared to $W10$ and WE.

In the third iteration, no channel breakdown issue, minimisation of the high subthreshold leakage current and smaller channel length modulation have been achieved from the *n*-channel devices. Thinner gate oxide, shallower junction depths for source/drain by reducing the furnace temperature and longer channels have been employed in order to reduce the influence of drain voltage on the channel i.e. the second order effect.



(a) $I_{ds} - V_{ds}$ characteristics



(b) $\sqrt{I_{ds}} - V_{gs}$ and transfer characteristics

Figure 6.6 *The DC measurements of the enhancement mode n-MOSFET with $L_c = 20\ \mu m$, $W_c = 60\ \mu m$ and t_{ox}~55 nm from wafer WF. (a) The $I_{ds} - V_{ds}$ characteristics showing the linear and saturation regimes. The channel length modulation within the device has been observed to be smaller compared to the first and second iterations. (b) The $\sqrt{I_{ds}} - V_{gs}$ characteristics and the transfer characteristics in the saturation regime at $V_{ds} = 5\ V$ measure $V_{th} = -1.5\ V$ and $g_m = 0.16\ mS$.*

The first order effect i.e. the substrate doping can also be manipulated in order to control the subthreshold current. The presence of high subthreshold current has been described previously to be due to the small/light boron substrate doping that promotes the formation of strong electrons inversion layer induced by Q_{ss} within the channel of the enhancement and depletion mode *n*-MOSFETs. The influence of Q_{ss} that induces the formation of strong electrons inversion layer can be minimised by increasing the boron substrate doping [87].

In our work, the presence of subthreshold current has been further minimised to $\sim\mu A$ range by employing the phosphorus substrate doping and creating the *p*-channel devices instead of *n*-channel. The elimination of the subthreshold current due to the reverse effect from the *p*-channel devices will be presented in Chapter 7.

6.3.4 Wafer mapping of threshold voltage variation for enhancement mode *n*-MOSFET

In this section, the variation of threshold voltage with respect to the X-Y position across the wafer has been investigated. The threshold voltage has been measured from the fabricated enhancement mode *n*-MOSFETs which have been distributed on 32 different chips across the whole wafer as shown in Figure 6.7. The devices have been fabricated in two wafers, labelled as Wafer A and Wafer B. The 3-inch boron-doped $< 100 >$ silicon wafers with the nominal bulk resistivity of $\rho = 14\,\Omega cm - 20\,\Omega cm$ have been used. The devices have been created using the same fabrication process described for WE.

Previously, small variation of threshold voltage from $-3\,V$ to $-4\,V$ has been measured from the fabricated enhancement mode *n*-MOSFETs in wafer WE, as the measured devices are on the same chip. Larger variations of the threshold voltage have been measured across the wafers and mapped in Figure 6.8.

In Figure 6.8(a), the measured threshold voltage across Wafer A is within the range of $-5\,V$ to $-15\,V$. The enhancement mode *n*-MOSFETs situated close to the bottom of Wafer A have been found to have higher negative threshold voltage compared to

the other parts of the wafer. In Figure 6.8(b), a smaller range of threshold voltage from $-4\,V$ to $-7\,V$ has been measured across Wafer B. The devices close to the centre of Wafer B have been found to have higher negative threshold voltage compared to other parts.

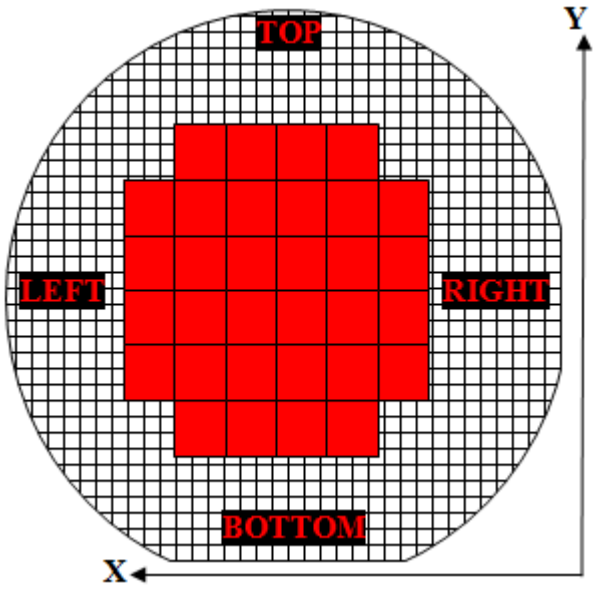
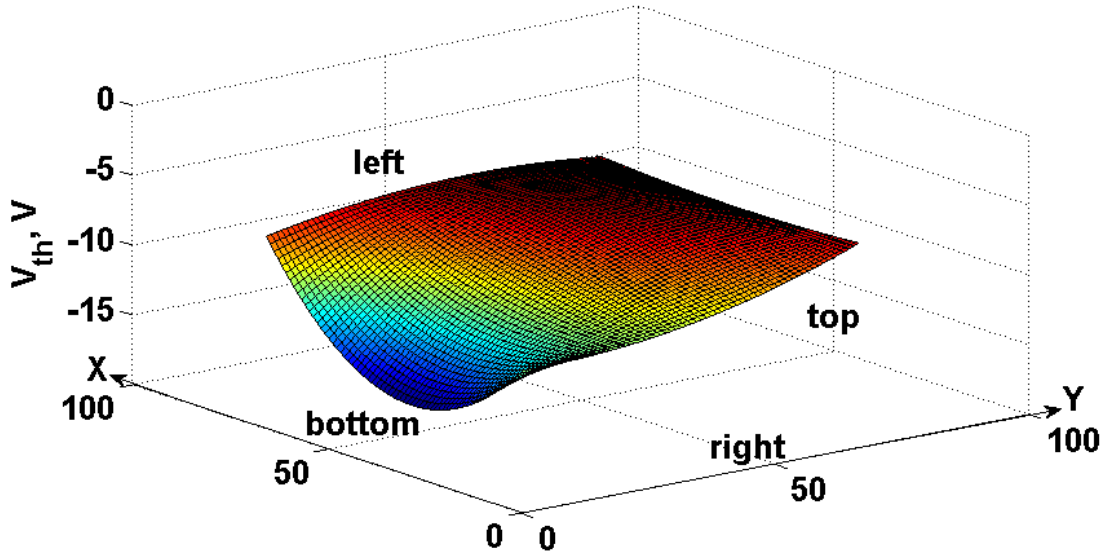
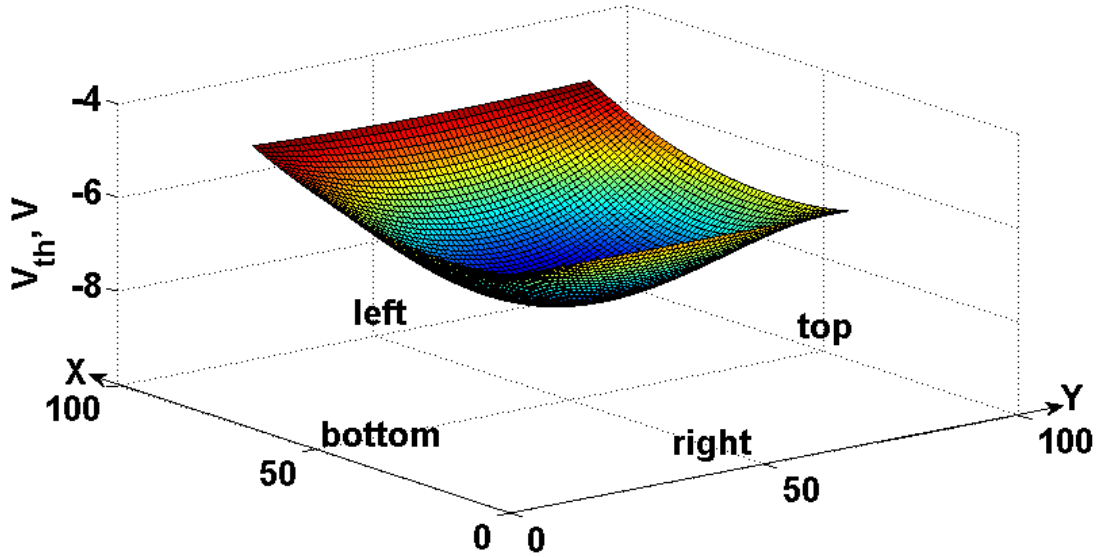


Figure 6.7 *The enhancement mode n-MOSFETs are fabricated at* 32 *different chips across the* 3 *–inch boron-doped* $< 100 >$ *silicon wafer according to the X-Y coordinates.*

There are 3 factors that have been suspected to cause the variation of threshold voltage for the fabricated enhancement mode *n*-MOSFETs across a wafer and also between different wafers. 1) The non-uniformity of boron surface concentration across the wafer might have caused the observed variation in the threshold voltage of the devices. Smaller boron concentration N_A within the silicon channel surface can make the threshold voltage to become more negative [equation 5.1]. 2) In addition, the thickness of gate oxide layer depends on the doping of the substrate [48]. The non-uniformity of the grown gate oxide thickness across the wafer due to the non-uniform boron surface concentration can also contribute to the variation of the threshold voltage. 3) The third factor that can cause this variation is the quality of the grown gate oxide layer. From equation 5.1, a higher Q_{ss} value within the gate oxide can lead to a more negative value of threshold voltage.



(a) Wafer A



(b) Wafer B

Figure 6.8 *The measurement and mapping of the threshold voltage variation from the enhancement mode n-MOSFET devices fabricated across (a) Wafer A and (b) Wafer B.*

6.4 The fabrication of *n*-RGT

The source/drain regions and *n*-type enhancement mode channels have been integrated with the metal bridge gate structures to form the *n*-channel resonant gate transistors (*n*-RGTs). The aluminium bridge gate structure of length $l_b = 92\ \mu m$ has been integrated with the source/drain regions and *n*-type enhancement mode channel

developed in wafer WE to create the *n*-channel resonant aluminium gate transistor (*n*-RAGT). Meanwhile, the developed source/drain regions and *n*-type enhancement mode channel from wafer WF have been integrated with the tantalum bridge gate structure of length $l_b = 92\ \mu m$ and $l_b = 278\ \mu m$ to create the *n*-channel resonant tantalum gate transistor (*n*-RTGT).

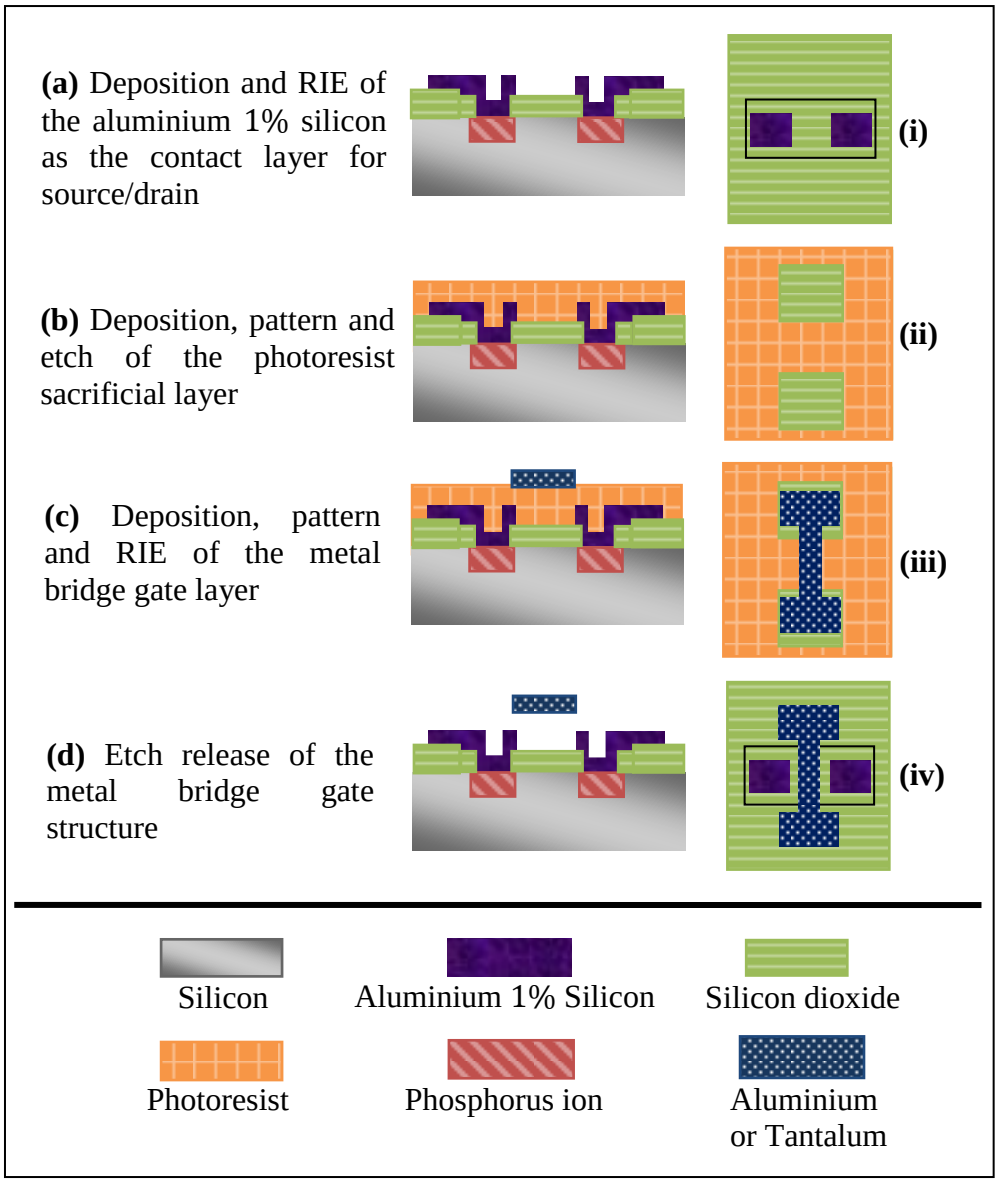


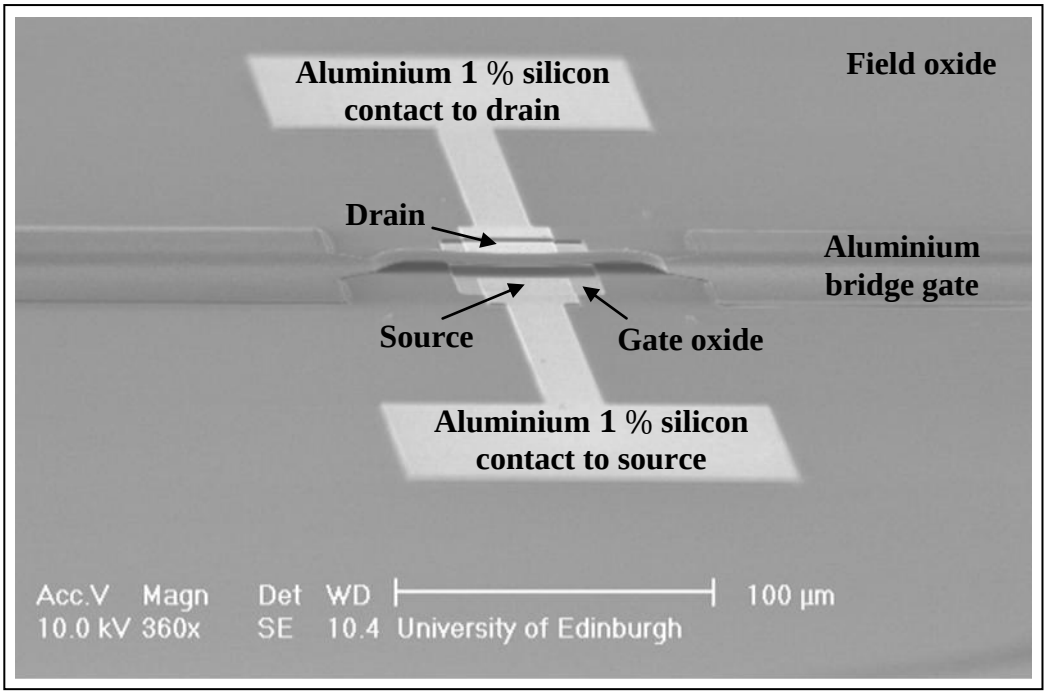
Figure 6.9 *The integration of source/drain regions and n-type enhancement mode channel with the aluminium or tantalum bridge gate structure for the fabrication of the n-RAGT or n-RTGT. [(a)-(d)] The cross sectional view and [(i)-(iv)] the top view of the fabrication process.*

In Figure 6.9, the steps for fabricating the *n*-RAGT and *n*-RTGT are shown. The fabrication parameters for the implantation of source/drain regions and for the growth of gate oxide layer on a 3-inch boron-doped silicon substrate have been described in detail in section 5.3 in Chapter 5. The formation of aluminium 1% silicon electrode contact to the phosphorus implanted source/drain regions is shown in Figure 6.9(a)(i).

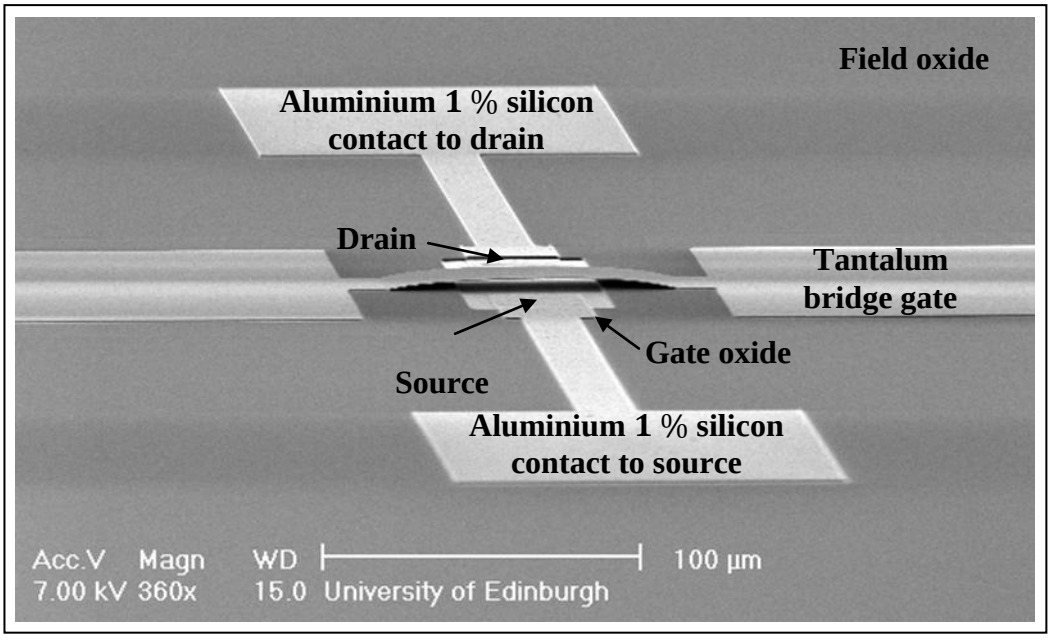
The photoresist sacrificial layer of $\sim 4\,\mu m$ thickness has been deposited onto the wafer and patterned photolithographically in order to define the areas for the anchors of the bridge gate [Figure 6.9(b)(ii)]. The sacrificial layer has been baked on a hot plate for $30\ minutes$ at 200 ℃ in order to vaporise out all moisture within the layer. The sacrificial layer thickness defines the distance of the bridge gate from the channel region.

After the photoresist sacrificial layer baking step, the aluminium or tantalum metal layer of $0.5\,\mu m$ thickness has been sputter-deposited onto the wafer, patterned photolithographically and etched using the reactive ion etching technique (RIE) to define the shape of the metal bridge gate structure [Figure 6.9(c)(iii)]. After the metal etching step, the photoresist mask has been removed in oxygen plasma and the 3-inch wafer has been diced into $1\,cm \times 1\,cm$ chips. Finally, the photoresist sacrificial layer has been removed with an etch release process using the downstream oxygen/nitrogen plasma tool, releasing the metal bridge gate as the overlying free-standing structure on top of the channel region [Figure 6.9(d)(iv)].

The SEM micrograph images of the fabricated *n*-RGT structures with the bridge length of $l_b = 92\ \mu m$ are shown in Figure 6.10. For the fabricated *n*-RAGT in wafer WE, the distance from aluminium bridge gate to the substrate has been measured to be $d_i \sim 4\ \mu m$ in Figure 6.10(a). The etch release process has been considered to be clean as there is no residue from the photoresist sacrificial layer left on the substrate. The released aluminium bridge gate structure is seen to have a considerably straight profile above the channel region. The fabricated *n*-RTGT from wafer WF is shown in Figure 6.10(b). The tantalum bridge gate has been observed to buckle upwards.



(a) *n*-RAGT



(b) *n*-RTGT

Figure 6.10 *The SEM micrograph images of the fabricated (a) n-RAGT and (b) n-RTGT with the channel length of $L_c = 20\ \mu m$, channel width of $W_c = 40\ \mu m$ and the bridge gate length of $l_b = 92\ \mu m$. The corresponding air gap distance from the bridge gate to the channel region has been measured to be $d_i \sim 4\ \mu m$ and $d_i \sim 7\ \mu m$, respectively.*

Thus, the air gap distance from the tantalum bridge gate to the substrate has been made unintentionally bigger than the initial deposited thickness of the photoresist sacrificial layer. The maximum central vertical deflection of the tantalum bridge gate has been measured to be $d_i \sim 7\ \mu m$ above the channel region in Figure 6.10(b).

6.5 DC measurement of *n*-RGT

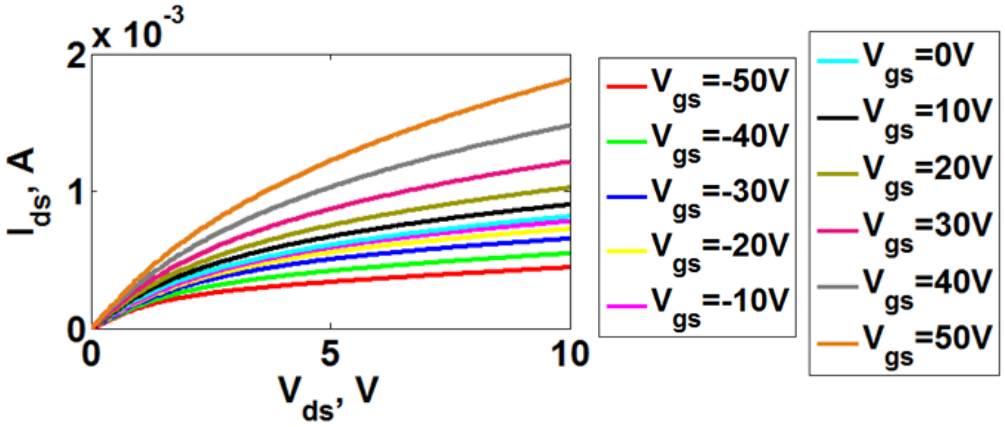
The threshold voltage and transconductance of the fabricated *n*-RGT devices have been measured and compared with their *n*-MOSFET counterparts/equivalents. From the comparison, the effects of introducing the air gap spacing between the bridge gate and channel region have been analysed.

6.5.1 Threshold voltage and transconductance of *n*-RAGT

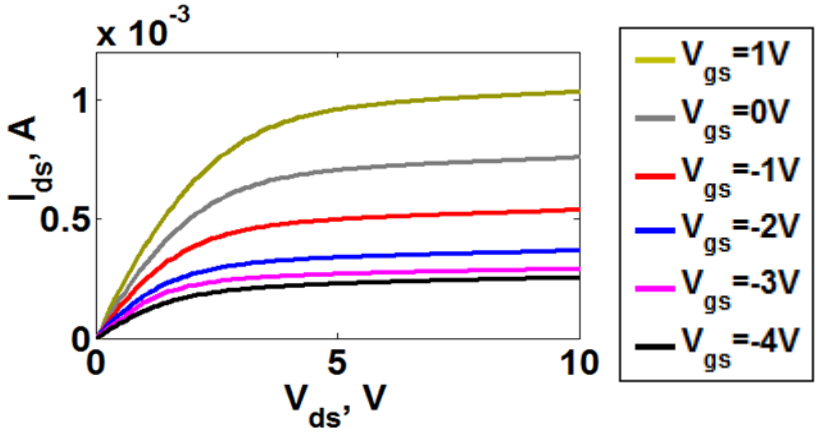
The $I_{ds} - V_{ds}$ characteristics measured from the *n*-RAGT with channel length of $L_c = 10\ \mu m$, channel width of $W_c = 60\ \mu m$, bridge gate length of $l_b = 92\ \mu m$, air gap spacing of $d_i \sim 4\ \mu m$ and gate oxide thickness of $t_{ox} \sim 77\ nm$ have been plotted in Figure 6.11(a). For comparison, the measured $I_{ds} - V_{ds}$ characteristics for the *n*-MOSFET of similar geometrical dimensions have been plotted in Figure 6.11(b). The characteristics and performance of the channel for the *n*-RAGT is assumed to be similar with the one measured from the *n*-MOSFET. The only difference between these two devices is the insertion of air gap of a certain distance between the bridge gate and the channel region. In order to increase the accuracy of the comparison, the fabricated *n*-RAGT and *n*-MOSFET in wafer WE have been measured from the same chip.

In Figure 6.11(a), the operating bridge gate voltage for the enhancement mode *n*-RAGT is $V_{gs} = -50\ V$ to $+50\ V$ with $V_{ds} = 0\ V - 10\ V$. The threshold voltage of the device has been estimated to be $V_{th} = -50\ V$ with the subthreshold current of $I_{th} \sim 0.4\ mA$. The maximum transconductance in the saturation regime has been measured to be $g_m = 35\ \mu S$. In addition, the pull-in voltage for the *n*-RAGT has been measured to be $V_{pi} \sim 60\ V$. Therefore, the operation limit for the bridge gate voltage of *n*-RAGT has been restricted between the pull-in voltage of the aluminium

bridge gate structure and the threshold voltage of the channel i.e. $-50\,V < V_{gs} < +60\,V$.



(a) *n*-RAGT



(b) *n*-MOSFET

Figure 6.11 *The comparison of the $I_{ds} - V_{ds}$ characteristics measured between the enhancement mode (a) n-RAGT and (b) n-MOSFET fabricated in wafer WE with $L_c = 10\,\mu m$, $W_c = 60\,\mu m$, d_i~4 μm, $l_b = 92\,\mu m$ and t_{ox}~77 nm.*

The $I_{ds} - V_{ds}$ characteristics measured from the enhancement mode *n*-MOSFET with the gate voltage varies from $-4\,V$ to $1\,V$ is shown in Figure 6.11(b). The threshold voltage has been measured to be $-4\,V$ with the subthreshold current of I_{th}~0.4 mA. The maximum transconductance in the saturation regime has been measured to be $g_m = 290\,\mu S$. As has been discussed previously, the trapped positive oxide charges Q_{ss} within the gate oxide layer have caused the fabricated

enhancement mode *n*-MOSFET and *n*-RAGT devices to possess the depletion mode characteristics.

From the comparison between the enhancement mode *n*-RAGT and *n*-MOSFET, 1) the transconductance for *n*-RAGT has been measured to be one order less than *n*-MOSFET, indicating smaller modulation of channel conductance in *n*-RAGT. 2) The threshold voltage for *n*-RAGT has been found to be one order higher than *n*-MOSFET. The smaller transconductance and higher threshold voltage for *n*-RAGT compared to *n*-MOSFET are related to the presence of the air gap layer of $\sim 4\ \mu m$ thickness on top of the $77\ nm$ thickness of gate oxide layer.

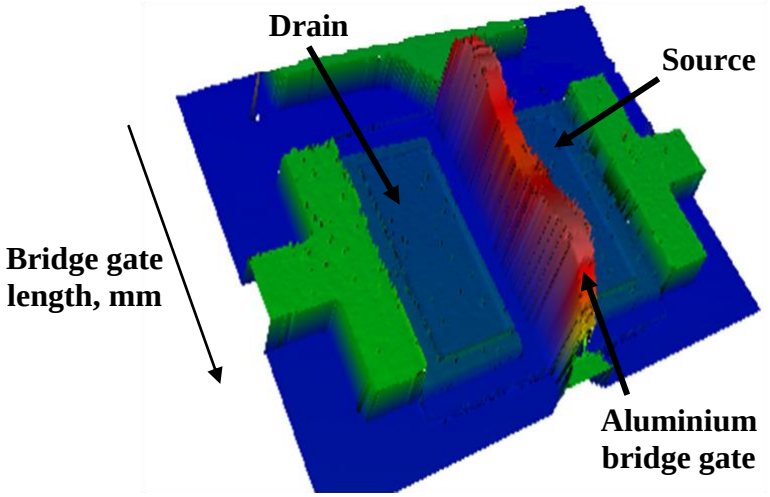
The influence of air gap layer on the $I_{ds} - V_{ds}$ characteristics of RGT has been modelled using PSpice in section 7.5.1 in Chapter 7. Basically, the total capacitance between the aluminium bridge gate and channel of *n*-RAGT is dominated by the air capacitance of $C_{air} \sim 2.2\ \mu F/m^2$ while the estimated total capacitance in *n*-MOSFET is $C_{ox} \sim 450\ \mu F/m^2$. From equation 2.20, smaller total capacitance in *n*-RAGT has made the transconductance value to be smaller than *n*-MOSFET.

The threshold voltage has been described in equation 5.1 to depend on the distance of the metal gate from the silicon channel surface. In *n*-RAGT, higher electric field induced by the bridge gate is required to turn the device on/off and modulate the channel conductance compared to the condition when the bridge gate is on the channel region. Thus, the threshold voltage in *n*-RAGT is higher than *n*-MOSFET.

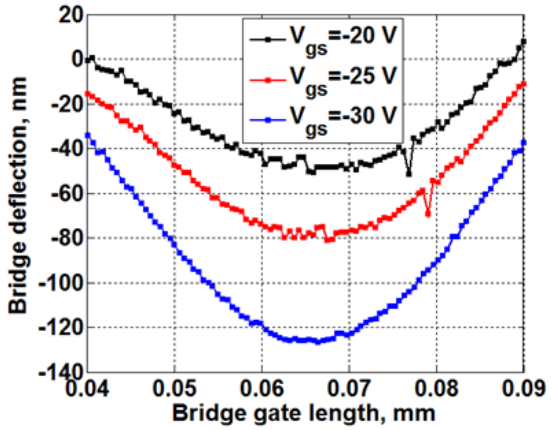
6.5.1.1 Electromechanical response of *n*-RAGT

In section 2.4.4.2 in Chapter 2, the voltage applied onto the bridge gate V_{gs} has been described to influence the electromechanical behaviour of the RGT device. The induced attractive electrostatic force between the bridge gate and channel increases as the applied V_{gs} increases. Thus, the bridge gate undergoes a small deflection that reduces the air gap spacing. The deflection of aluminium bridge gate structure in the *n*-RAGT device with the bridge gate length of $l_b = 92\ \mu m$ due to the induced

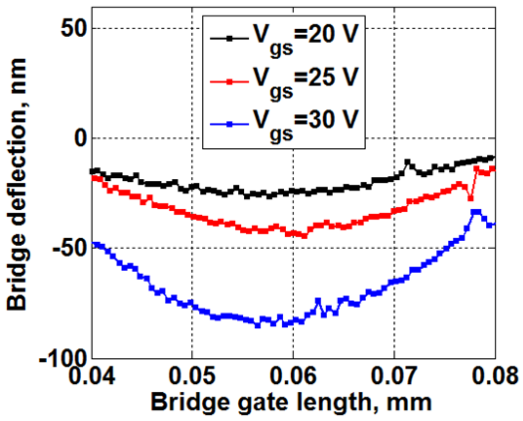
electrostatic force between the bridge gate and channel has been measured using the interferometric profilometry.



(a) Aluminium bridge gate deflection



(b) Negative bridge gate voltage regime



(c) Positive bridge gate voltage regime

Figure 6.12 *(a) The deflection of aluminium bridge gate structure for the n-RAGT device due to the induced attractive electrostatic force is measured using the interferometric profilometry. The downwards bridge gate deflections are measured at* $V_{ds} = 5\ V$ *and* V_{gs} *varied from (b)* $0\ V$ *to* $-30\ V$ *for negative bridge gate voltage regime and (c)* $0\ V$ *to* $+30\ V$ *for positive bridge gate voltage regime.*

Figure 6.12(a) shows the scanned image of the *n*-RAGT device under the influence of the attractive electrostatic force due to the applied bridge gate voltage V_{gs}. A constant drain to source voltage of $V_{ds} = 5\ V$ has been applied on the device while

the bridge gate voltage has been varied from $V_{gs} = -30\,V$ to $+30\,V$. The operation for *n*-RAGT has been categorised into two different bridge gate voltage regimes. There are the negative bridge gate voltage regime and the positive bridge gate voltage regime. The middle section of the aluminium bridge gate structure has been measured to deflect downwards in both regimes.

The measurement of the aluminium bridge gate deflections as the applied bridge gate voltage increases have been plotted in Figure 6.12(b) for the negative bridge gate voltage regime of $V_{gs} = 0\,V$ to $-30\,V$ and in Figure 6.12(c) for the positive bridge gate voltage regime of $V_{gs} = 0\,V$ to $+30\,V$. In both regimes, the induced downwards deflection has been measured to increase as the applied bridge gate voltage increases. The maximum central downwards deflections of $25\,nm - 125\,nm$ have been measured from the devices which brings down the bridge gate structure to be closer to the channel.

In Figure 6.13, the applied $V_{gs} = +30\,V$ onto the bridge gate will enhance the electrons inversion layer within the channel. The net surface potential at the channel region which consists of the positive oxide charges Q_{ss} and electrons inversion layer will become more negative than the applied $V_{gs} = +30\,V$. Thus, the induced electric field and electrostatic force between the aluminium bridge gate and channel region will pull the bridge gate towards the channel. Conversely, the applied $V_{gs} = -30\,V$ onto the bridge gate will deplete the electrons inversion layer within the channel. As the net surface potential at the channel region becomes more positive than the applied $V_{gs} = -30\,V$, the induced electric field and electrostatic force between the aluminium bridge gate and channel region will pull the bridge gate towards the channel.

The decrease in air gap spacing between the aluminium bridge gate and the channel region of *n*-RAGT has been suspected to 1) contribute to the increase in modulation of channel conductance for both positive and negative bridge gate voltage regimes. As the bridge gate is pulled to be much closer to the channel, the enhancement and

depletion of the electrons inversion layer by the bridge gate will be more effective. 2) In addition, the threshold voltage of the channel will also become smaller with respect to the decrease in distance of the aluminium bridge gate from the silicon channel surface as the applied bridge gate voltage increases.

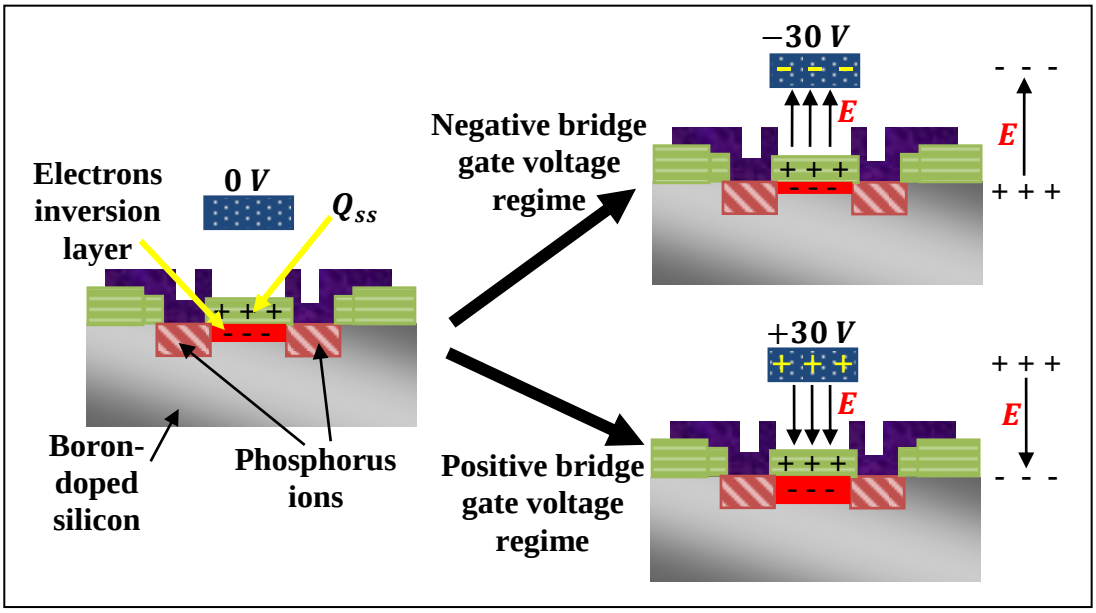


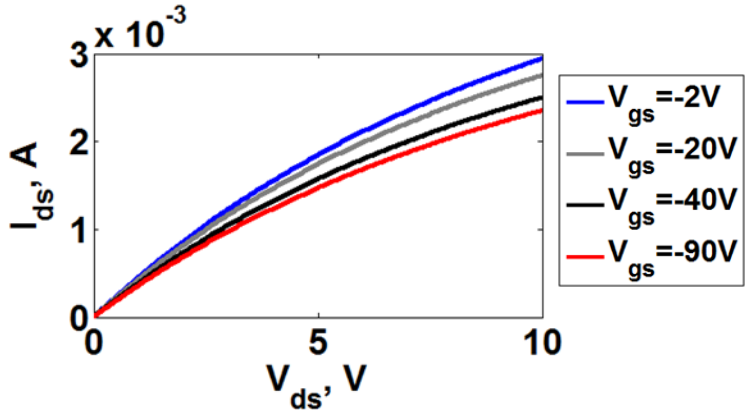
Figure 6.13 *The attractive electrostatic force acted between the aluminium bridge gate structure and the channel region of n-RAGT in positive and negative bridge gate voltage regimes has deflected the bridge gate towards the channel region.*

6.5.2 Threshold voltage and transconductance of *n*-RTGT

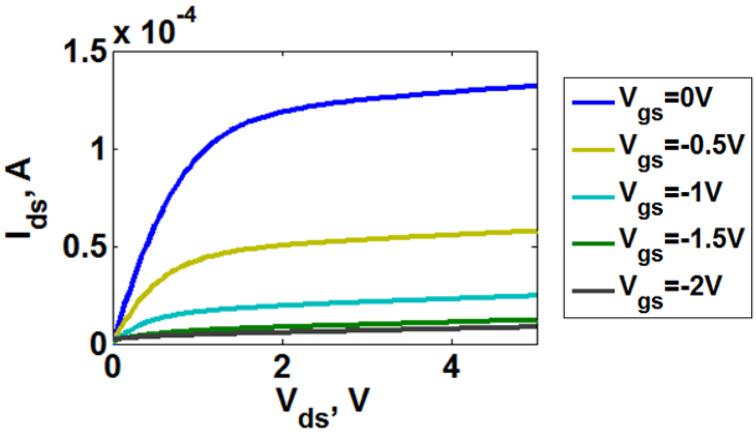
From wafer WF, the $I_{ds} - V_{ds}$ characteristics for the enhancement mode *n*-RTGT with channel length of $L_c = 20\,\mu m$, channel width of $W_c = 60\,\mu m$, bridge gate length of $l_b = 92\,\mu m$, air gap spacing of $d_i \sim 7\,\mu m$ and gate oxide thickness of $t_{ox} = 55\,nm$ have been measured and plotted in Figure 6.14(a). The operating bridge gate voltage for *n*-RTGT is $V_{gs} = -2\,V$ to $-90\,V$ with $V_{ds} = 0\,V - 10\,V$. The maximum transconductance from the maximum gradient of the transfer characteristics has been measured to be $g_m = 12.5\,\mu S$. In addition, the pull-in voltage for the *n*-RTGT has been measured to be $V_{pi} > 100\,V$.

For comparison, the $I_{ds} - V_{ds}$ characteristics for the enhancement mode *n*-MOSFET of similar geometrical dimensions have been measured and plotted in Figure 6.14(b)

with the gate voltage varies from $-2\,V$ to $0\,V$. The maximum transconductance has been measured to be $g_m = 160\,\mu S$. Smaller total capacitance in *n*-RTGT has made the transconductance value to be one order smaller than *n*-MOSFET.



(a) *n*-RTGT



(b) *n*-MOSFET

Figure 6.14 *The comparison of the $I_{ds} - V_{ds}$ characteristics measured between the enhancement mode (a) n-RTGT and (b) n-MOSFET fabricated in wafer WF with $L_c = 20\,\mu m$, $W_c = 60\,\mu m$, $l_b = 92\,\mu m$, d_i~$7\,\mu m$ and t_{ox}~$55\,nm$.*

From the interferometric profilometry measurement, the downwards deflection for the tantalum bridge gate of *n*-RTGT with the bridge gate length similar to the aluminium bridge gate of *n*-RAGT ($l_b = 92\,\mu m$) has been found to be very small and negligible with respect to the applied bridge gate voltage. The tantalum bridge gate possesses higher mechanical restoring force with higher air gap spacing of d_i~$7\,\mu m$ compared to the aluminium bridge gate of d_i~$4\,\mu m$. Therefore in *n*-

RTGT, smaller attractive electrostatic force has been induced on the tantalum bridge gate from the channel, leading to smaller bridge gate deflection.

Comparing the transconductance and $I_{ds} - V_{ds}$ characteristics measured for the *n*-RTGT in Figure 6.14(a) with the *n*-RAGT in Figure 6.11(a), smaller modulation of channel conductance has been observed from the *n*-RTGT due to the higher air gap spacing of $d_i \sim 7\ \mu m$ compared to the *n*-RAGT of $d_i \sim 4\ \mu m$. Thus, smaller total capacitance in *n*-RTGT has made the transconductance value to be smaller than *n*-RAGT.

6.5.2.1 Influence of bridge gate length and channel width on transconductance

In order to increase the modulation of channel conductance for the *n*-RTGT, longer tantalum bridge gate structure of $l_b = 278\ \mu m$ and bigger channel width of $W_c = 140\ \mu m$ have been employed. In equation 2.20, bigger channel width will give higher transconductance value i.e. higher modulation of channel conductance.

From the interferometric profilometry measurement, significant downwards deflection of the tantalum bridge gate has been observed with respect to the applied bridge gate voltage. Therefore, larger electromechanical deflection of the bridge gate has been achieved using 1) bigger channel width that induces larger attractive electrostatic force and 2) longer bridge gate structure with smaller mechanical restoring force. Larger bridge gate deflection reduces the distance of the bridge gate from the channel and subsequently helps to increase the modulation of channel conductance for the *n*-RTGT.

The $I_{ds} - V_{ds}$ characteristics for the enhancement mode *n*-RTGT with channel length of $L_c = 10\ \mu m$, channel width of $W_c = 140\ \mu m$, bridge gate length of $l_b = 278\ \mu m$, air gap spacing of $d_i \sim 13\ \mu m$ and gate oxide thickness of $t_{ox} \sim 55\ nm$ has been measured and plotted in Figure 6.15. The operating bridge gate voltage for the *n*-RTGT is from $V_{gs} = 0\ V$ to $-80\ V$ with $V_{ds} = 0\ V - 10\ V$. The threshold voltage from the device has been measured to be $V_{th} \sim -40\ V$ with the subthreshold current

of 1.2 mA. The maximum transconductance of $g_m = 41\ \mu S$ has been measured from the *n*-RTGT of $l_b = 278\ \mu m$, which is higher than the measured $g_m = 12.5\ \mu S$ from the *n*-RTGT of $l_b = 92\ \mu m$ in Figure 6.14(a), indicating that higher modulation of channel conductance has been obtained from the *n*-RTGT device of $l_b = 278\ \mu m$.

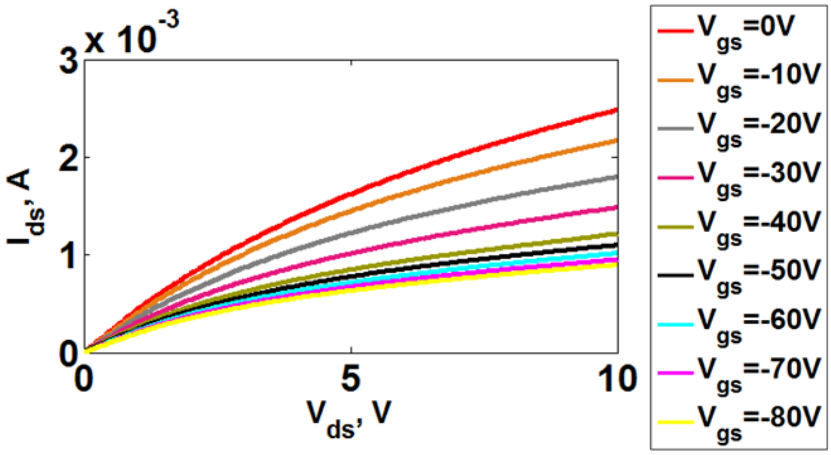


Figure 6.15 *The $I_{ds} - V_{ds}$ characteristics for the enhancement mode n-RTGT fabricated in wafer WF with $L_c = 10\ \mu m$, $W_c = 140\ \mu m$, $l_b = 278\ \mu m$, d_i~13 μm and t_{ox}~55 nm. Higher modulation of channel conductance has been achieved with $l_b = 278\ \mu m$ and $W_c = 140\ \mu m$ compared to $l_b = 92\ \mu m$ and $W_c = 60\ \mu m$ in Figure 6.14(a).*

6.5.3 Optimisation for RGT

The mechanical bridge gate structure and channel for the resonant gate transistor need to be optimised in order for the device to be more sensitive electromechanically. For the bridge gate, the structure needs to be placed close to the channel region so that higher modulation of channel conductance could be achieved from the device.

For the *n*-type channel, the presence of high subthreshold current has been seen to be a major problem that reduces the modulation of channel conductance. The second order effect has been minimised in the *n*-MOSFET devices by increasing the influence of the perpendicular electric field from the gate. In *n*-RGT device however, the influence of the perpendicular electric field from the bridge gate is small due the presence of air gap layer. Thus, the depletion and enhancement of the

channel conductance by the bridge gate voltage has become less effective. High subthreshold current has been measured from the RGT devices.

The presence of high subthreshold current has been described to be induced by the built-in positive oxide charges Q_{ss}. In Chapter 7, the effect of positive oxide charges has been reversed by employing the *p*-type channel for the resonant gate transistor, eliminating the high subthreshold current. Therefore, the *p*-channel resonant gate transistors have been measured with better modulation of channel conductance compared to the *n*-channel resonant gate transistors.

6.6 Conclusion

In this chapter, the enhancement and depletion mode *n*-MOSFETs have been fabricated and measured. The enhancement mode *n*-MOSFETs have been measured to possess the depletion mode characteristics, probably due to the influence of the positive oxide charges on the channel. The transconductance increased from $g_m = 0.38\ mS$ to $4.46\ mS$ with the increase of channel width to channel length ratio from $\frac{W_c}{L_c} = 2.5$ to 54. High subthreshold currents, close to $1\ mA$ have been measured within the enhancement mode *n*-MOSFETs. The presence of high subthreshold current has been observed to reduce the strength in modulation of the channel conductance. For depletion mode *n*-MOSFETs, the subthreshold currents have been measured to be higher than $1\ mA$ and for devices of $\frac{W_c}{L_c} > 8$, channel breakdown occurred.

The effects of increasing the $\frac{W_c}{L_c}$ ratio for the enhancement and depletion mode *n*-MOSFETs have been found to 1) increase the number of devices with channel breakdown to 40 % for the enhancement mode and 90% for the depletion mode and 2) increase the subthreshold currents for the enhancement mode to be higher than $1\ mA$. In order to resolve these issues, 1) the channel length has been increased from $L_c \leq 10\ \mu m$ to $20\ \mu m$, 2) the furnace temperatures used to anneal the phosphorus implanted source/drain regions and during the growth of gate oxide layer have been

reduced to 14 % and 3) the gate oxide thickness has been reduced to 25 %. These optimisations have minimised the subthreshold current to ~90 % and eliminated the occurrence of channel breakdown within the *n*-MOSFET devices.

The aluminium bridge gate structure of length $l_b = 92\ \mu m$ has been integrated with the n-type channel of width $W_c = 60\ \mu m$ to become *n*-RAGT with the measured air gap distance of $d_i \sim 4\ \mu m$. The fabricated aluminium bridge gate structure is considerably straight/flat. Comparing the performance of *n*-RAGT with its *n*-MOSFET equivalent, the effects of inserting an air gap layer between the aluminium bridge gate and channel region have been found to 1) reduce the transconductance to one order less and 2) increase the threshold voltage to one order higher. The aluminium bridge gate has been induced to deflect towards the channel and the deflection increased with the increase of positive or negative bridge gate voltages.

The tantalum bridge gate structure of length $l_b = 92\ \mu m$ has been integrated with the n-type channel of width $W_c = 60\ \mu m$ to become *n*-RTGT with the measured air gap distance of $d_i \sim 7\ \mu m$. The fabricated tantalum bridge gate has been observed to buckle upwards. Compared to the *n*-RAGT, the induced downwards deflection of the tantalum bridge gate structure has been found to be negligible with respect to the applied bridge gate voltages and the modulation of channel conductance has been measured to be 60 % smaller due to $d_i \sim 7\ \mu m$. Longer tantalum bridge gate of $l_b = 278\ \mu m$ and bigger channel width of $W_c = 140\ \mu m$ have been employed to induce larger tantalum bridge gate deflection which reduces d_i and subsequently increases the transconductance.

Chapter 7: The measurement and characterisation of *p*-MOSFET and *p*-RGT

7.1 Introduction

In this chapter, the boron implanted source/drain regions and the enhancement mode *p*-type channel will be developed. The enhancement mode *p*-channel metal-oxide-semiconductor field-effect transistor (*p*-MOSFET) will be fabricated and measured for the development of the enhancement mode *p*-channel resonant gate transistor (*p*-RGT). The created boron implanted source/drain regions and the enhancement mode *p*-type channel will be integrated with the tantalum bridge gate structure, forming the enhancement mode *p*-channel resonant tantalum gate transistor (*p*-RTGT).

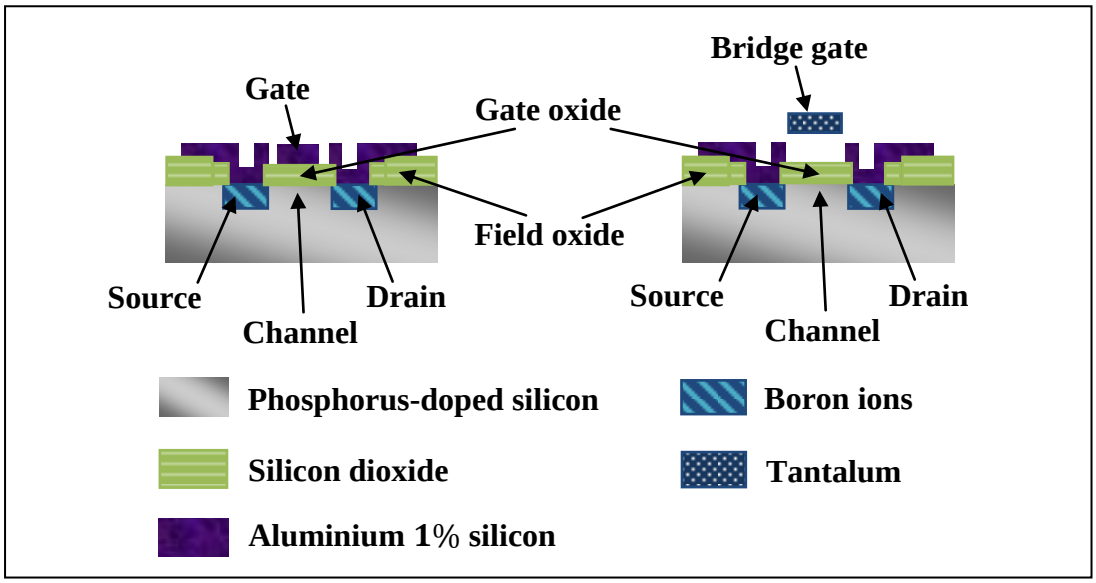
The threshold voltage and transconductance for *p*-MOSFETs and *p*-RTGTs will be measured and compared. The effects of introducing an air gap spacing between the tantalum bridge gate and *p*-type channel region on the transconductance of *p*-RTGT will be analysed and modelled. The performance of the fabricated enhancement mode *p*-channel devices will be compared with the enhancement mode *n*-channel devices measured in Chapter 6. The reverse effect of the positive oxide charges Q_{ss} due to the employed *p*-type channel will be demonstrated by the elimination of the high subthreshold current.

The influence of channel width and channel length on the transconductance of the *p*-channel devices will be investigated. The electromechanical behaviour of the *p*-RTGTs at different tantalum bridge gate length will be addressed. The voltage

operating limits for the tantalum bridge gate of *p*-RTGT will be measured. Finally, the tuning of the tantalum bridge gate vibration within the audible frequency range will be demonstrated.

7.2 The operation of *p*-channel devices

The enhancement mode *p*-channel metal-oxide-semiconductor field-effect transistor (*p*-MOSFET) requires the *n*-type silicon wafer as the substrate and *p*-type ion implantation for source/drain regions. The cross sectional view for the enhancement mode *p*-MOSFET is shown in Figure 7.1(a). The *n*-type phosphorus-doped < 100 > silicon wafer has been chosen as the substrate while boron ions have been implanted as the *p*-type dopants for the source/drain regions.



(a) *p*-MOSFET **(b)** *p*-RTGT

Figure 7.1 *The cross sectional views of the enhancement mode (a) p-MOSFET and (b) p-RTGT. Aluminium* 1% *silicon has been employed as the gate for the p-MOSFET while tantalum as the bridge gate for the p-RTGT.*

In Figure 7.1(b), the tantalum bridge gate structure is integrated with the enhancement mode *p*-type channel and boron implanted source/drain regions in order to form the enhancement mode *p*-channel resonant tantalum gate transistor (*p*-RTGT). The enhancement mode *p*-MOSFET and *p*-RTGT require negative DC bias

voltage V_{gs} to be applied onto the gate and tantalum bridge gate in order to form the holes inversion layer within the silicon channel surface and obtain the drain current conduction. The enhancement mode *p*-channel devices work with the opposite current and voltage polarities to the enhancement mode *n*-MOSFET and *n*-RTGT devices described in Chapter 6.

7.3 The fabrication process

The steps for fabricating the *p*-MOSFET and *p*-RTGT are depicted in Figure 7.2. The 3-inch phosphorus-doped $< 100 >$ silicon wafer with the nominal bulk resistivity of $\rho = 1\ \Omega cm - 10\ \Omega cm$ has been employed as the substrate. The silicon dioxide layer of $0.5\ \mu m$ thickness has been grown thermally onto the wafer as the field oxide. Reactive ion etching (RIE) using CF_4/H_2 plasma has been performed on the field oxide layer in order to define the active channel region of the device [Figure 7.2(a)(i)]. The next step is to grow the silicon dioxide layer as the gate oxide for the device. The gate oxide thickness of t_{ox}~$70\ nm$ has been grown thermally using the dry oxidation process at 1100 ℃ for $30\ minutes$ [Figure 7.2(b)(ii)].

Then, the source/drain regions have been patterned photolithographically onto the wafer before the implantation of boron [Figure 7.2(c)(iii)]. The photoresist acts as the masking layer during the implantation procedure. Boron ions of dose $1e^{14}\ ions/cm^2$ and energy $30\ keV$ have been implanted into the silicon substrate through the gate oxide layer [Figure 7.2(c)(iii)]. Compared to the fabrication process described previously for the *n*-MOSFET and *n*-RTGT, the implantations of source/drain regions for the *p*-MOSFET and *p*-RTGT have been performed after the growth of the gate oxide layer. This is due to the segregation of boron dopants which has been discussed in section 5.4.1.1 in Chapter 5. High furnace temperature of 1100 ℃ employed during dry oxidation process and annealing of the implantation regions have been simulated to deplete the boron surface concentration as the boron dopants segregate from the silicon substrate into the grown silicon dioxide layer. Thus, the implantation of boron has been performed after the gate oxidation process in order to minimise the boron segregation effect at the source/drain regions.

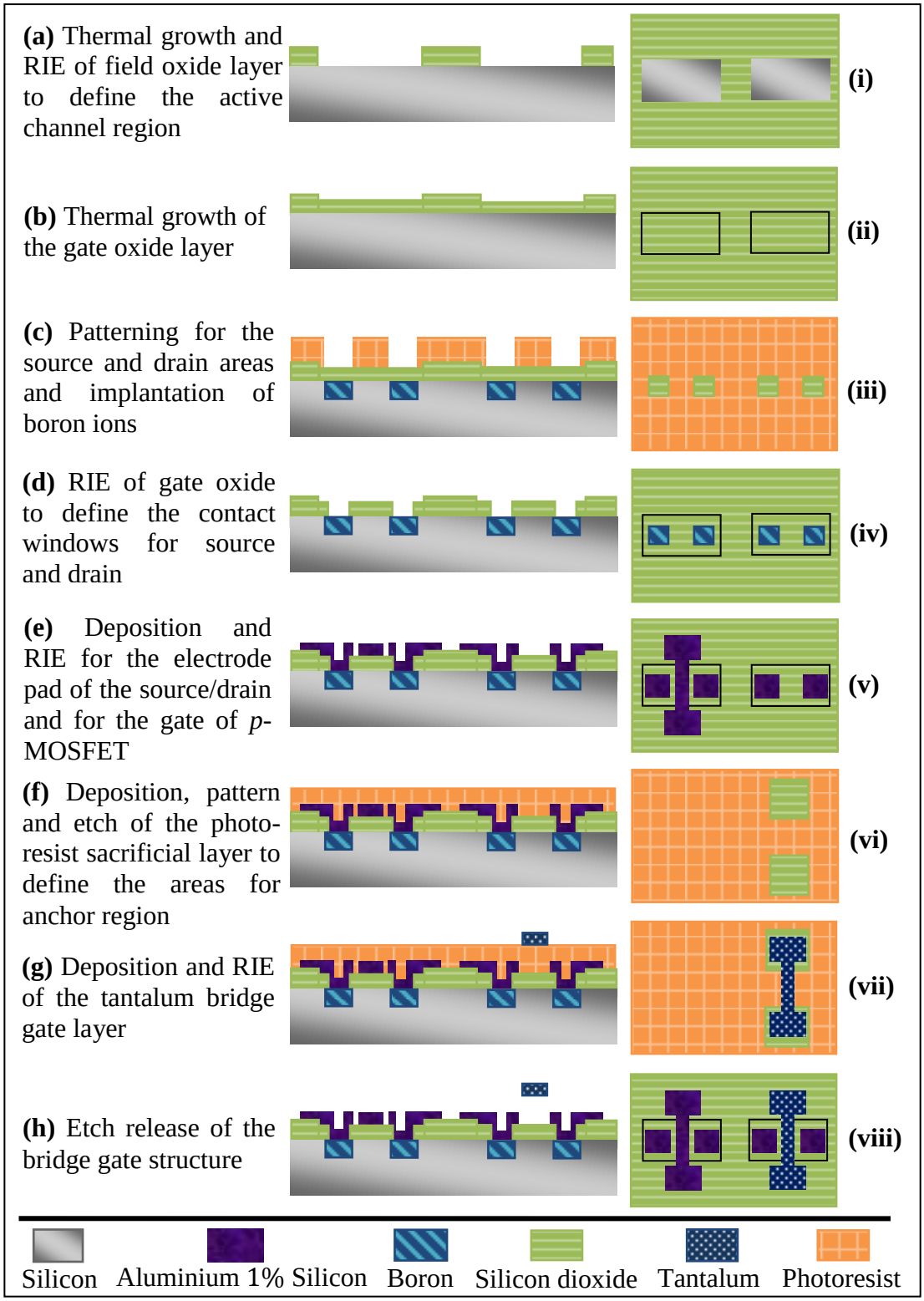


Figure 7.2 *[(a)-(h)] The cross sectional view and [(i)-(viii)] top view of the fabrication process for making the p-MOSFET and p-RTGT devices.*

After boron implantation, the photoresist masking layer has been removed in oxygen plasma and the wafer has been annealed at $1100\,℃$ for $25\,minutes$ to activate the implanted boron dopants. Next, RIE using CF_4/H_2 plasma has been performed on the gate oxide layer to open the interfacial contact windows [Figure 7.2(d)(iv)]. Aluminium 1% silicon of $0.5\,\mu m$ thickness has been sputter-deposited onto the wafer as the metalisation layer [Figure 7.2(e)(v)]. The boron implanted source/drain regions will be in contact with the metalisation layer through the interfacial contact windows. In Figure 7.2(e)(v), RIE using $SiCl_4$/Ar plasma has been carried out on the metalisation layer in order to define the electrode pad for the source/drain of *p*-MOSFET and *p*-RTGT and also for the gate of *p*-MOSFET.

Next, the tantalum bridge gate structure will be fabricated above the *p*-type channel. The photoresist sacrificial layer of $4\,\mu m$ thickness has been deposited and patterned photolithographically to define the areas for the anchor of the bridge gate [Figure 7.2(f)(vi)]. The sacrificial layer has been baked on a hot plate for $30\,minutes$ at $200\,℃$ in order to vaporise out all moistures within the layer. The photoresist sacrificial layer will also act as a masking layer to protect the *p*-MOSFET and the source/drain of *p*-RTGT from the subsequent processing steps. After the photoresist sacrificial layer baking step, the tantalum metal layer of $0.5\,\mu m$ thickness has been sputter-deposited onto the wafer and RIE using $SiCl_4$/Ar plasma has been carried out on the tantalum layer in order to define the shape of the bridge gate structure [Figure 7.2(g)(vii)]. After the metal etching step, the 3-inch wafer has been diced into $1\,cm \times 1\,cm$ chips. Finally, the photoresist sacrificial layer has been removed with an etch release process in the downstream oxygen/nitrogen plasma tool, releasing the metal bridge gate as the overlying free-standing structure on top of the channel region [Figure 7.2(h)(viii)]. The tantalum bridge gate structures have been released from the photoresist sacrificial layer under the etch release condition of $250\,℃$ substrate temperature and $2500\,sccm/500\,sccm$ oxygen/nitrogen gas flow rates.

In this study, the tantalum bridge gates of length $l_b = 0.092\,mm - 1.62\,mm$, thickness $t_b = 0.5\,\mu m$ and width $w_b = 10\,\mu m - 25\,\mu m$ have been fabricated. The

p-type channels have been designed with the channel length of $L_c = 10\ \mu m - 25\ \mu m$ and channel width of $W_c = 40\ \mu m - 160\ \mu m$. The width of the tantalum bridge gate w_b is the length of the channel L_c. In Figure 7.3, the SEM micrograph image of the fabricated *p*-RTGTs is shown. In the figure, six tantalum bridges gates of length $l_b = 1.62\ mm - 0.91\ mm$ and labelled as $B1 - B6$ have been integrated with six *p*-channels of $L_c \times W_c = 20\ \mu m \times 160\ \mu m$, forming the *p*-RTGTs. The tantalum bridge gates have been observed to buckle upwards with the maximum central vertical deflection increasing from $d_i \sim 34.4\ \mu m$ to $59.2\ \mu m$ with respect to the increase in the bridge gate length. The drive and sense circuitry made of aluminium 1 % silicon metalisation layer has been designed to connect each bridge gate, source and drain to the bond pads.

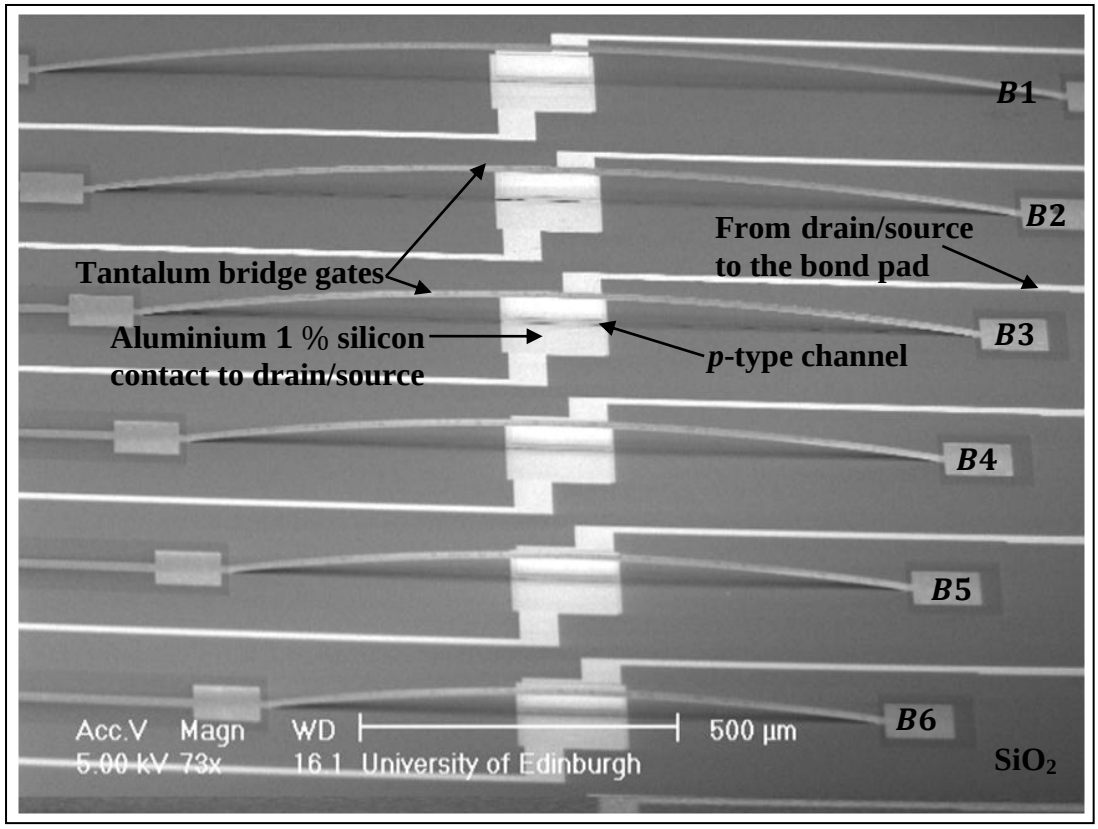


Figure 7.3 *The SEM micrograph image of the fabricated p-RTGTs. The tantalum bridge gates with $t_b = 0.5\ \mu m$, $w_b = 20\ \mu m$ and $l_b = 1.62\ mm - 0.91\ mm$ have been integrated with the p-type channels to create the p-RTGTs. The geometrical designs for the p-type channels are $L_c = 20\ \mu m$, $W_c = 160\ \mu m$ and $t_{ox} \sim 70\ nm$.*

7.4 DC measurement of the enhancement mode *p*-MOSFET and *p*-RTGT

The drain current I_{ds} has been measured from the fabricated *p*-channel devices by varying the drain voltage V_{ds} and the gate/bridge gate voltage V_{gs}, while the source and substrate terminals being grounded. The *p*-channel devices have been observed to operate within the linear and saturation regimes.

By employing the *p*-type channel, 100 % of the fabricated *p*-MOSFETs and *p*-RTGTs have been seen to be free from the presence of high subthreshold currents which have been measured previously from the *n*-channel devices in Chapter 6. The influence of positive oxide charges Q_{ss} that induces the formation of electrons inversion layer within the silicon channel surface and causes the high subthreshold current within the *n*-channel devices has been eliminated by the use of *p*-type channel.

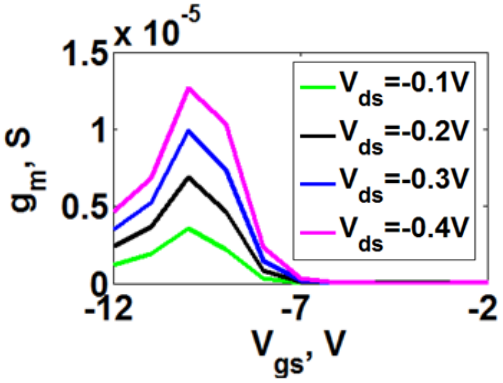
7.4.1 Small subthreshold current in *p*-MOSFET

The DC measurement results of the enhancement mode *p*-MOSFET with t_{ox}~70 nm, $L_c = 15\ \mu m$ and $W_c = 80\ \mu m$ are shown in Figure 7.4. The threshold voltage V_{th} has been extracted from the linear and saturation regimes of the device by extrapolating the transconductance curves in Figure 7.4(a) and the $\sqrt{I_{ds}} - V_{gs}$ characteristics in Figure 7.4(b) to the V_{gs} axis. The threshold voltage has been measured to be $V_{th} \sim -6.5\ V$.

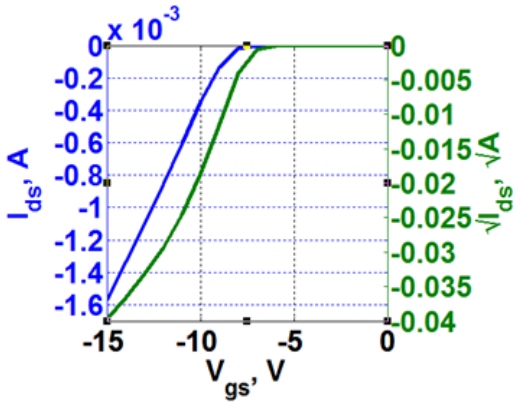
From the $I_{ds} - V_{gs}$ transfer characteristics in the saturation regime plotted in Figure 7.4(b), a small subthreshold current of $I_{th} \sim -8.7\ \mu A$ has been measured at $V_{th} \sim -6.5\ V$. The maximum transconductance from the maximum gradient of the transfer characteristics has been measured to be $g_m = 236\ \mu S$ at $|V_{gs}| = |V_{th}| + 9\ V$ and $V_{ds} = -20\ V$.

The $I_{ds} - V_{ds}$ characteristics have been plotted in Figure 7.4(c), showing the linear and saturation regimes of the device. The drain current in the saturation regime

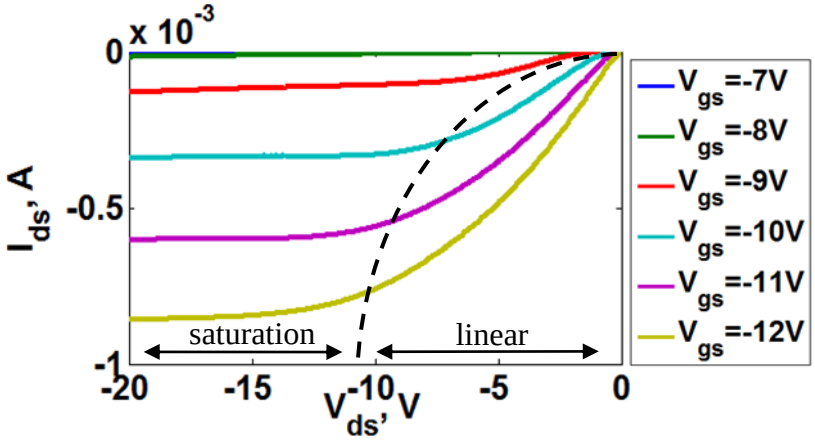
increases from I_{ds}~0 μA to $-850\ \mu A$ as the gate voltage increases from $V_{gs} = -7\ V$ to $-12\ V$. Compared to the fabricated *n*-MOSFETs in Chapter 6, the measured drain current from the fabricated *p*-MOSFET is one order smaller. This might be due to the fact that the charge carriers in *p*-channel devices are holes and the effective carrier mobility for holes is smaller than the effective carrier mobility for electrons in the *n*-channel devices by a factor of 2 to 4 [104]. The *p*-MOSFET has been observed to enter the saturation regime when $|V_{ds}| > |V_{gs}| - |V_{th}|$.



(a) Transconductance curves



(b) $\sqrt{I_{ds}} - V_{gs}$ and transfer characteristics

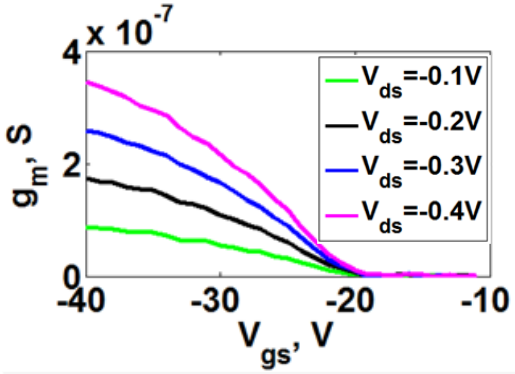


(c) $I_{ds} - V_{ds}$ characteristics

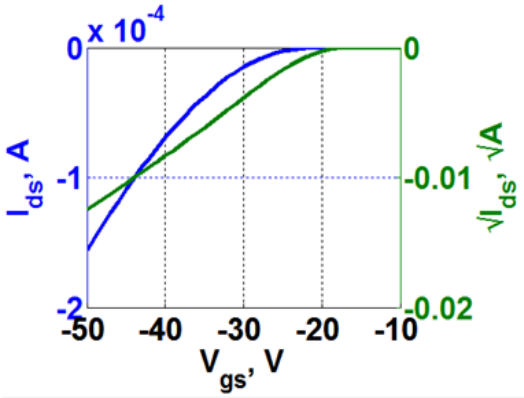
Figure 7.4 *The DC measurement of the enhancement mode p-MOSFET with $L_c = 15\ \mu m$, $W_c = 80\ \mu m$ and t_{ox}~70 nm. (a) The $g_m - V_{gs}$ characteristics in the linear regime measure V_{th}~$-6.5\ V$. (b) The $\sqrt{I_{ds}} - V_{gs}$ characteristics and the transfer characteristics in the saturation regime at $V_{ds} = -20\ V$ measure V_{th}~$-6.5\ V$ and $g_m = 236\ \mu S$. (c) The $I_{ds} - V_{ds}$ characteristics with small subthreshold current of I_{th}~$-8.7\ \mu A$ has been measured.*

7.4.2 Small subthreshold current in *p*-RTGT

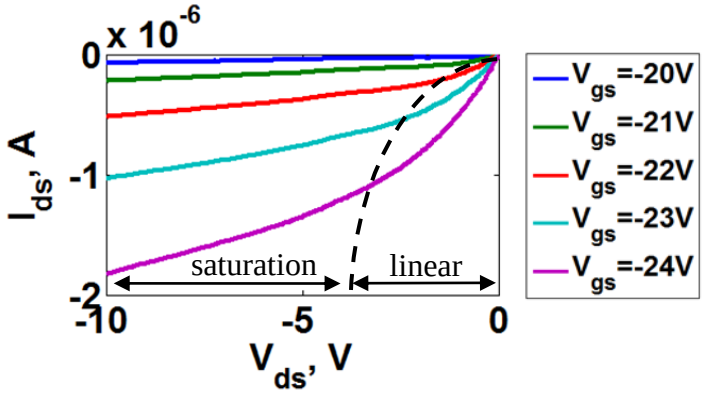
The DC measurement results of the enhancement mode *p*-RTGT with $l_b = 92\ \mu m$, d_i~$7\ \mu m$, t_{ox}~$70\ nm$, $L_c = 15\ \mu m$ and $W_c = 80\ \mu m$ are shown in Figure 7.5. The threshold voltage of $V_{th} \sim -20\ V$ has been measured from the linear [Figure 7.5(a)] and saturation regimes [Figure 7.5(b)] of the device.



(a) Transconductance curves



(b) $\sqrt{I_{ds}} - V_{gs}$ and transfer characteristics



(c) $I_{ds} - V_{ds}$ characteristics

Figure 7.5 *The DC measurement of the enhancement mode p-RTGT with $l_b = 92\ \mu m$, d_i~$7\ \mu m$, $L_c = 15\ \mu m$, $W_c = 80\ \mu m$ and t_{ox}~$70\ nm$. (a) $g_m - V_{gs}$ characteristics in the linear regime measure $V_{th} \sim -20\ V$ (b) The $\sqrt{I_{ds}} - V_{gs}$ characteristics and the transfer characteristics in the saturation regime at $V_{ds} = -10\ V$ measure $V_{th} \sim -20\ V$ and $g_m = 10\ \mu S$ (c) The $I_{ds} - V_{ds}$ characteristics with small subthreshold current of $I_{th} \sim -75\ nA$ has been measured.*

From Figure 7.5(b), a small subthreshold current of $I_{th} \sim -75\ nA$ has been measured at $V_{th} \sim -20\ V$. The maximum transconductance has been measured to be $g_m =$

$10\ \mu S$ at $|V_{gs}| = |V_{th}| + 30\ V$ and $V_{ds} = -10\ V$. The $I_{ds} - V_{ds}$ characteristics of the device has been plotted in Figure 7.5(c), showing the increase of drain current in the saturation regime from $I_{ds} \sim 0\ \mu A$ to $-1.9\ \mu A$ as the gate voltage increases from $V_{gs} = -20\ V$ to $-24\ V$. The enhancement mode *p*-RTGT has been observed to enter the saturation regime when $V_{ds} = V_{gs} - V_{th}$. The measured drain current in the saturation regime is not constant but increases as a function of V_{ds} at a constant value of V_{gs}, indicating the presence of channel length modulation within the fabricated device.

Compared to the fabricated enhancement mode *p*-MOSFET of similar geometrical dimensions, the transconductance for the enhancement mode *p*-RTGT is one order less while the threshold voltage is one order higher. The measured discrepancies are related to the presence of the air gap layer of $\sim 7\ \mu m$ thickness on top of the $\sim 70\ nm$ thickness of gate oxide layer.

7.5 The analytical model for drain current of the enhancement mode *p*-MOSFET and *p*-RTGT

In the previous section, the transconductance of the enhancement mode *p*-RTGT have been measured and compared with its *p*-MOSFET equivalent. Both devices have been fabricated on the same chip with similar channel dimensions. The only physical difference between *p*-RTGT and *p*-MOSFET is the presence of an air gap layer between the tantalum bridge gate structure and the channel region of *p*-RTGT.

The analytical static drain current model and the corresponding $I_{ds} - V_{ds}$ characteristics have been created for the *p*-MOSFET. From the fitting of the $I_{ds} - V_{ds}$ characteristics model for *p*-MOSFET to the measurement, the effective surface holes mobility of the device, μ_h has been estimated. Similarly, the drain current model and the corresponding $I_{ds} - V_{ds}$ characteristics for *p*-RTGT have been created using the estimated μ_h value from the *p*-MOSFET model. By fitting the $I_{ds} - V_{ds}$ characteristics model of *p*-RTGT to its measured data, the total capacitance C_{total} between the channel and the tantalum bridge gate structure of *p*-RTGT has

been estimated. Therefore, the influence of air gap layer on the transconductance of *p*-RTGT can be quantified.

In drain current model and measurement, constant air gap spacing has been assumed. C_{total} can be estimated with better accuracy by employing the tantalum bridge gate length of $l_b = 92\ \mu m$, as the bridge gate deflection at this length with respect to the applied V_{gs} is very small. Thus, the air gap distance of d_i~$7\ \mu m$ remains fixed with respect to the applied V_{gs} in order for the drain current model to apply.

7.5.1 The analytical drain current model

The theoretical approximations of the static drain current for the enhancement mode *p*-MOSFET are shown in equation 7.1 for the linear regime (for $|V_{gs}| > |V_{th}|$ and $|V_{ds}| \leq |V_{gs}| - |V_{th}|$) and equation 7.2 for the saturation regime (for $|V_{gs}| > |V_{th}|$ and $|V_{ds}| \geq |V_{gs}| - |V_{th}|$), where $K_n = \mu_h C_{total} \frac{W_c}{L_c}$ and λ is the channel length modulation parameter that quantifies the influence of V_{ds} on the drain current I_{ds} when the device is in saturation. C_{total} is the total capacitance per unit area between the channel and the gate/bridge gate. For *p*-MOSFET, C_{total} quantifies the capacitance within the gate oxide layer C_{ox}, while for *p*-RTGT, C_{total} is the series capacitance of the air gap layer C_{air} and the gate oxide layer C_{ox}.

$$I_{ds} = K_n \left[(V_{gs} - V_{th}) V_{ds} - \frac{{V_{ds}}^2}{2} \right] (1 + \lambda V_{ds}) \tag{7.1}$$

$$I_{ds} = \frac{K_n}{2} (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}) \tag{7.2}$$

μ_h represents the effective surface mobility of holes within the *p*-type channel. The bulk mobilities of the charge carriers within the silicon substrate have been reported to be $1300\ cm^2/Vs$ for electrons and $500\ cm^2/Vs$ for holes at $300\ K$ [87]. The effective surface mobilities of the charge carriers within the channel inversion layer differ from the bulk values. Leistiko *et al* have reported on the measured mobilities for both electrons and holes within the channel inversion layer to be approximately a

half of their bulk mobilities [87]. The typical value of the effective surface holes mobility in transistors is $\mu_h = 250\ cm^2/Vs$ [104].

7.5.1.1 Estimation of effective surface holes mobility from I_{ds}-V_{ds} characteristics model of *p*-MOSFET

The measurement of $I_{ds} - V_{ds}$ characteristics for *p*-MOSFET has been shown previously in Figure 7.4(c). The $I_{ds} - V_{ds}$ characteristics model for the device has been simulated using PSpice and plotted together with the measurement in Figure 7.6. The effective surface holes mobility of $\mu_h = 200\ cm^2/Vs$ has been estimated from the fitting of the $I_{ds} - V_{ds}$ characteristics model to the measurement, using $L_c = 15\ \mu m$, $W_c = 80\ \mu m$, $\lambda = 0\ V^{-1}$ and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \sim 490\ \mu F/m^2$, with ε_{ox} and t_{ox} being the permittivity and thickness of the gate oxide layer.

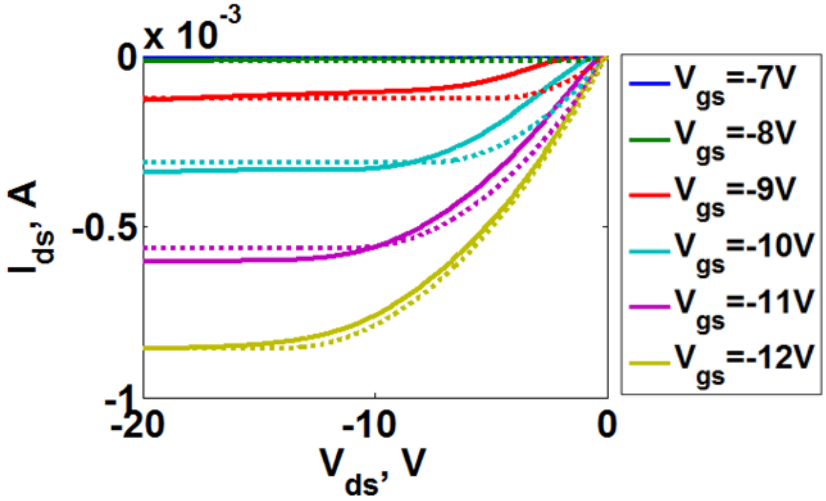


Figure 7.6 *The measurement (solid lines ▬) and the approximate model (dotted lines ▪▪▪) of the $I_{ds} - V_{ds}$ characteristics for p-MOSFET with $L_c = 15\ \mu m$, $W_c = 80\ \mu m$ and $t_{ox} \sim 70\ nm$. The effective surface holes mobility of $\mu_h = 200\ cm^2/Vs$ has been extracted from the fitting.*

From Figure 7.6, the voltage applied onto the gate has been swept from $V_{gs} = -7\ V$ to $-12\ V$. In the beginning, the onset of drain current conductions measured at $V_{gs} = -9\ V$, $-10\ V$ and $-11\ V$ are delayed in the linear regime and then the device saturated at higher drain currents compared to the model in the saturation regime.

The measured drain currents in the linear regime have been observed to be non-linear. At $V_{gs} = -12\,V$, the measured drain current has stabilised and agreed well with the model. The device has been observed to stabilise within the linear and saturation regimes as the applied gate voltage increases.

7.5.1.2 Estimation of total capacitance from I_{ds}-V_{ds} characteristics model of *p*-RTGT

Next, the $I_{ds} - V_{ds}$ characteristics model for the *p*-RTGT which has been measured previously in Figure 7.5(c) has been simulated and plotted in Figure 7.7 using the estimated $\mu_h = 200\ cm^2/Vs$. At $V_{gs} = -24\,V$, the measured drain current I_{ds} in the saturation regime increases with the increase of V_{ds} at the rate of $\sim 0.13\ \mu A/V$. The corresponding drain-source shunt resistance has been measured to be $r_{ds} \sim 7.5\ M\Omega$ and the channel length modulation parameter, λ of the device has been estimated to be $\lambda = 1/r_{ds} I_{ds(sat)} \sim 0.12\ V^{-1}$. The effect of channel length modulation, $\lambda = 0.12\ V^{-1}$ has been included in the $I_{ds} - V_{ds}$ characteristics model for *p*-RTGT.

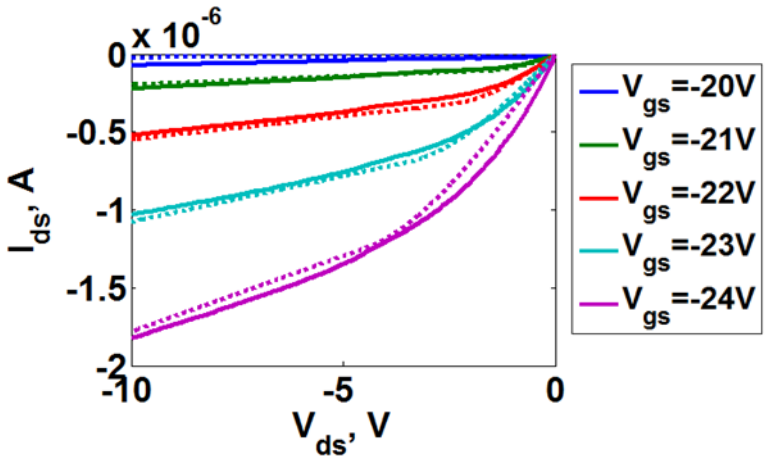


Figure 7.7 *The measurement (solid lines ▬) and the approximate model (dotted lines ▪▪▪) of the $I_{ds} - V_{ds}$ characteristics for p-RTGT with $l_b = 92\ \mu m$, $d_i \sim 7\ \mu m$, $L_c = 15\ \mu m$, $W_c = 80\ \mu m$ and $t_{ox} \sim 70\ nm$. The total capacitance of $C_{total} = 1.0\ \mu F/m^2$ has been extracted from the fitting.*

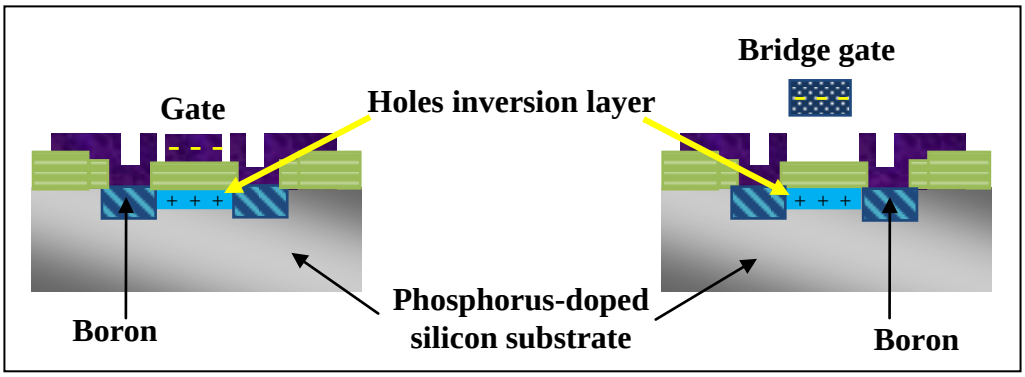
By fitting the $I_{ds} - V_{ds}$ characteristics model to the measurement in Figure 7.7, C_{total} has been estimated to be $1.0\ \mu F/m^2$. The estimated C_{total} is approximately

equal to the air gap capacitance of $C_{air} = \frac{\varepsilon_{air}}{d_i} \sim 1.2\ \mu F/m^2$. This indicates that the air gap capacitance dominates the total capacitance between the channel to the bridge gate. Based on equation 2.20 in Chapter 2, the vast decrease of the total capacitance in *p*-MOSFET from $\sim 490\ \mu F/m^2$ to the total capacitance of $\sim 1.0\ \mu F/m^2$ in *p*-RTGT has been suspected to reduce the measured transconductance of the *p*-RTGT to one order smaller than the *p*-MOSFET.

7.6 The analytical model for threshold voltage of the enhancement mode *p*-MOSFET

In the enhancement mode *p*-channel devices, the majority carrier within the *n*-type phosphorus-doped silicon substrate is electrons. In Figure 7.8, the negative DC bias voltage applied onto the gate/bridge gate will repel the electrons and attract the minority carriers i.e. holes towards the silicon channel surface. The holes concentration density is controlled by the perpendicular surface electric field exerted by the aluminium 1 % silicon gate/tantalum bridge gate.

At threshold voltage, the induced holes within the channel possess the concentration that exceeds the electron concentration density [85]. The silicon channel surface has been inverted from *n*-type to *p*-type and the induced holes inversion layer connects the source to drain for current conduction.



(a) *p*-MOSFET **(b)** *p*-RTGT

Figure 7.8 *The formation of holes inversion layer within the silicon channel surface of the (a) p-MOSFET and (b) p-RTGT with* $|V_{gs}| \geq |V_{th}|$.

7.6.2 Estimation of positive oxide charges from threshold voltage model of *p*-MOSFET

In this section, the threshold voltage equation for *p*-MOSFET is described. Using the measured threshold voltage from the *p*-MOSFET, the built-in positive oxide charges Q_{ss} is estimated from the equation. The threshold voltage of *p*-MOSFET is dependent on 1) the phosphorus doping concentration N_D at the silicon channel surface, 2) the presence of positive oxide charges Q_{ss} within the gate oxide at the gate oxide-silicon channel interface, 3) the work function of the material used for the gate and 4) the distance of silicon channel surface from the metal gate i.e. thickness of gate oxide t_{ox}. The threshold voltage of the *p*-MOSFET is represented by equation 7.3 [85][86];

$$V_{th} \approx -2\varphi_f - \frac{Q_B}{C_{ox}} + \varphi_{MS} - \frac{Q_{ss}}{C_{ox}} \tag{7.3}$$

where φ_{MS} is the work function difference between the metal gate and silicon channel surface, φ_f is the equilibrium electrostatic potential within the substrate, Q_B is the total charge stored per unit area within the depletion region and Q_{ss} is the total positive oxide charges per unit area.

For the *n*-type substrate, φ_f is given in equation 7.4 where $V_t = 25.9\,mV$ at $300\,K$ and η_i is the intrinsic carrier concentration of the silicon substrate;

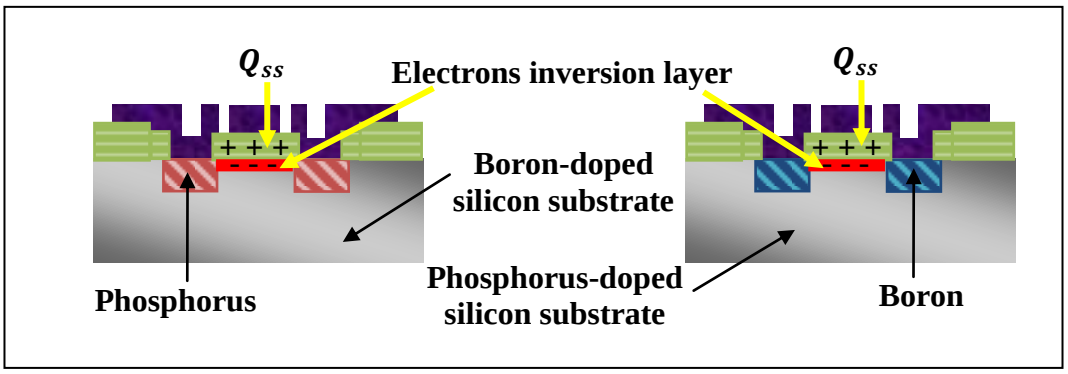
$$\varphi_f = V_t \ln\left(\frac{N_D}{\eta_i}\right) \tag{7.4}$$

Using aluminium 1% silicon as the gate, the value of φ_{MS} has been estimated to be $-0.31\,eV$. Deal *et al* have measured the metal-silicon work function to be $\varphi_{MS} \sim -0.3\,eV$ for aluminium – silicon dioxide – phosphorus-doped silicon substrate of $N_D \sim 10^{15}\,cm^{-3}$ at $300\,K$ [87][111]. Q_B is found from equation 7.5 with ε_{si} being the permittivity of the silicon substrate and $q = 1.6e^{-19}\,C$ [85][86].

$$Q_B = \sqrt{2\varepsilon_{si} q N_D \left|-2\varphi_f\right|} \tag{7.5}$$

Assuming $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \sim 490\ \mu F/m^2$, the expected negative threshold voltage for the enhancement mode *p*-MOSFET with $Q_{ss} = 0$ has been calculated from equation 7.3 to be $-1.2\ V$ which is much smaller than the measured value of $V_{th} = -6.5\ V$ in Figure 7.4.

In Chapter 6, the presence of Q_{ss} within gate oxide has been described to induce the formation of electrons inversion layer within the channel at gate voltage of $V_{gs} = 0\ V$. In enhancement mode *n*-MOSFET, the formation of electrons inversion layer at $V_{gs} = 0\ V$ has developed the depletion characteristics within the device. In Figure 7.9(a), the enhancement mode *n*-MOSFET is shown to be always on due to the presence of electrons inversion layer induced by Q_{ss}. Boron segregation/light boron doping at the silicon channel surface (the first order effect) formed stronger electrons inversion layer, causing high subthreshold leakage current problem.



(a) *n*-MOSFET **(b)** *p*-MOSFET

Figure 7.9 *The influence of positive oxide charges Q_{ss} on the channel of the enhancement mode (a) n-MOSFET and (b) p-MOSFET at $V_{gs} = 0\ V$. Depletion mode characteristic is developed within the enhancement mode n-MOSFET while higher gate voltage is needed for the enhancement mode p-MOSFET in order to create the holes inversion layer.*

The influence of Q_{ss} on the channel is reversed for the *p*-type channel devices. In the enhancement mode *p*-MOSFET [Figure 7.9(b)], the formation of electrons inversion layer due to Q_{ss} has caused the silicon channel surface to change from the lightly doped n^- to become heavily doped n^+. Extra internal reverse bias has been

developed within the channel which must be overcome in order to create the holes inversion layer [87]. Therefore, the enhancement mode *p*-MOSFET is always off and requires higher gate voltage in order to induce the formation of holes inversion layer and obtain drain current conduction [87].

Overall, the reverse effect of Q_{ss} has eliminated the presence of high subthreshold leakage current in the enhancement mode *p*-MOSFET and increased the threshold voltage required to turn on the device from the calculated value of $-1.2\,V$ to the measured value of $-6.5\,V$. From the threshold voltage equation, the estimated built–in positive oxide charges within the gate oxide layer for $V_{th} = -6.5\,V$ is $Q_{ss} = q(1.6e^{12})\,cm^{-2}$. Compared to the enhancement mode *n*-MOSFET, the estimated Q_{ss} in the enhancement mode *p*-MOSFET is higher, indicating that stronger electrons inversion layer has been developed within the *p*-type channel.

7.7 Further electrical/electromechanical characterisation of the enhancement mode *p*-MOSFET and *p*-RTGT

In this section, further characterisations have been performed on the fabricated *p*-channel devices. First, the variation of threshold voltage for the enhancement mode *p*-MOSFETs which have been fabricated across a wafer has been measured and mapped. Then, the effects of varying the channel width and channel length on the transconductance of the enhancement mode *p*-MOSFETs have been studied. For the enhancement mode *p*-RTGTs, the effects of varying the channel width and tantalum bridge gate length on the transconductance, threshold voltage and pull-in voltage have been presented.

7.7.1 Electrical characterisation of *p*-MOSFET

The enhancement mode *p*-MOSFETs with channel length of $L_c = 10\,\mu m$ and channel width of $W_c = 80\,\mu m$ have been fabricated across a wafer. The threshold voltages have been measured and mapped with respect to the position of the devices on the wafer. Then, the channel width and channel length for *p*-MOSFETs have been varied from $40\,\mu m$ to $140\,\mu m$ and $15\,\mu m$ to $25\,\mu m$, respectively. The

corresponding transconductance of the devices with respect to the change in channel width and length have been characterised.

7.7.1.1 Wafer mapping of threshold voltage variation for enhancement mode *p*-MOSFET

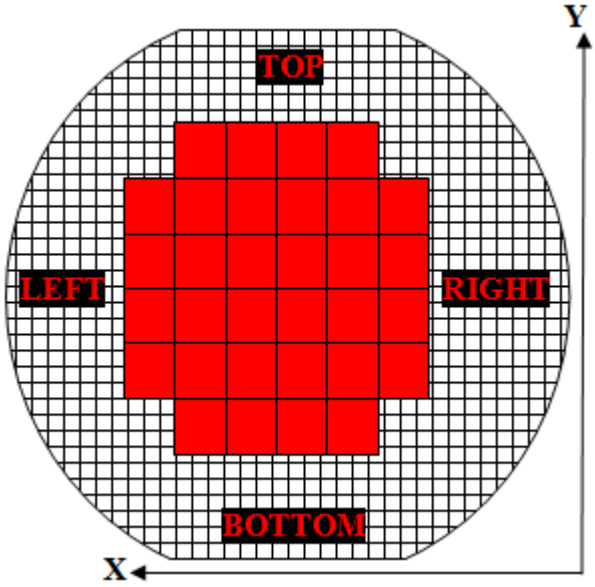
The variation of threshold voltage with respect to the X-Y position across the wafer has been measured in Figure 7.10. The enhancement mode *p*-MOSFETs have been fabricated and distributed on 32 different chips across the 3-inch phosphorus-doped $< 100 >$ silicon wafer with the nominal bulk resistivity of $\rho = 1\ \Omega cm - 10\ \Omega cm$ [Figure 7.10(a)]. The estimated average phosphorus surface concentration is $N_D \sim 1e^{15}\ atoms/cm^3$. The mapping of threshold voltage across the wafer in Figure 7.10(b) shows that the measured threshold voltage varies from $-3\ V$ to $-13\ V$. The *p*-MOSFETs which are situated close to the bottom and right sides of the wafer possess higher negative threshold voltage compared to the other parts of the wafer.

Similar with the wafer mapping of the threshold voltage variation for the enhancement mode *n*-MOSFETs in section 6.3.4, three factors have been suspected to cause the variation in threshold voltage for the enhancement mode *p*-MOSFETs across the wafer. 1) The non-uniformity of phosphorus surface concentration across the wafer might have caused the observed variation in the threshold voltage of the devices. Higher phosphorus surface concentration N_D can make the threshold voltage to become more negative [equation 7.3]. 2) The non-uniformity of the grown gate oxide thickness across the wafer due to the non-uniform phosphorus surface concentration can also contribute to the variation of the threshold voltage. 3) The third factor is the quality of the grown gate oxide layer. From equation 7.3, higher Q_{ss} within the gate oxide can lead to a more negative threshold voltage.

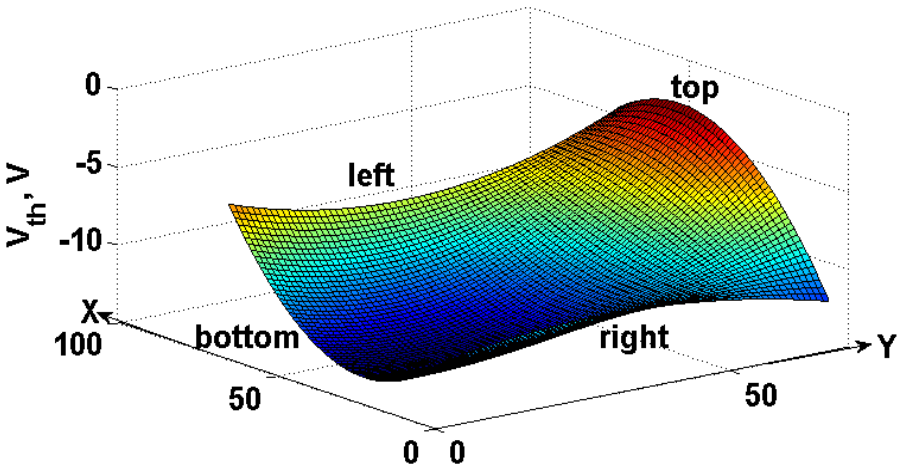
7.7.1.2 Influence of channel width and channel length on transconductance

The effect of increasing the size of channel width W_c and channel length L_c on the transconductance g_m of the *p*-MOSFETs has been studied. For $L_c = 15\ \mu m$ [Table

7.1(a)], the transconductance at $|V_{gs}| = |V_{th}| + 5\,V$ and $V_{ds} = -15\,V$ has been measured to increase from $59.2\,\mu S$ to $286.0\,\mu S$ when W_c increases from $40\,\mu m$ to $140\,\mu m$. The average threshold voltage has been measured from the devices to be $V_{th} \sim -4.5 \pm 1.5\,V$.



(a) The positions of 32 chips



(b) The wafer mapping profile of the threshold voltage variation

Figure 7.10 *(a) The enhancement mode p-MOSFETs are distributed at* 32 *different chips across the* 3*-inch phosphorus-doped* $< 100 >$ *silicon wafer according to the X-Y coordinates. (b) The mapping of the measured threshold voltage across the wafer shows a variation from* $-3\,V$ *to* $-13\,V$.

W_c	40	60	80	100	120	140
$g_m\ (\mu S)$	59.2	120.5	147.1	175.9	245.7	286.0
$V_{th}\ (V)$	-6	-6	-6	-3	-4	-3

(a) $L_c = 15\ \mu m$

W_c	40	60	80	100	120	140
$g_m\ (\mu S)$	50.4	73.0	118.7	137.6	170.2	201.0
$V_{th}\ (V)$	-6	-5	-5	-5	-5	-5

(b) $L_c = 20\ \mu m$

W_c	40	60	80	100	120	140
$g_m\ (\mu S)$	30.1	56.9	80.7	123.0	136.0	169.0
$V_{th}\ (V)$	-5	-4	-5	-3	-3	-3

(c) $L_c = 25\ \mu m$

Table 7.1 *The measured transconductance and threshold voltage for the enhancement mode p-MOSFETs of channel length (a) $L_c = 15\ \mu m$, (b) $L_c = 20\ \mu m$ and (c) $L_c = 25\ \mu m$ and a variation of channel width from $W_c = 40\ \mu m$ to 140 μm. The measured transconductance increases with respect to the decrease of channel length and increase of channel width.*

Conversely, as the channel length increases from $L_c = 15\ \mu m$ to $L_c = 25\ \mu m$, the transconductance has been measured to decrease. The range of transconductance for $L_c = 20\ \mu m$ is $50.4\ \mu S - 201.0\ \mu S$ with $V_{th} \sim -5 \pm 1\ V$ [Table 7.1(b)] while for $L_c = 25\ \mu m$, the transconductance has been measured within $30.1\ \mu S - 169.0\ \mu S$ with $V_{th} \sim -4.0 \pm 1\ V$ [Table 7.1(c)]. The measurement results are as predicted by equation 2.20 in which the transconductance increases with respect to the decrease of channel length and increase of channel width.

7.7.2 Electromechanical characterisation of *p*-RTGT

The channel width has been increased from $W_c = 40\ \mu m$ to $80\ \mu m$ for the enhancement mode *p*-RTGTs with the tantalum bridge gate length of $l_b = 92\ \mu m$

and from $W_c = 100\,\mu m$ to $140\,\mu m$ for the tantalum bridge gate length of $l_b = 278\,\mu m$. The corresponding threshold voltage, transconductance and pull-in voltage of the devices have been characterised. Then, the size of the channel region has been fixed to $L_c \times W_c = 20\,\mu m \times 160\,\mu m$. The effects of increasing the tantalum bridge gate length from $l_b = 0.57\,mm$ to $1.62\,mm$ on the pull-in voltage and threshold voltage of the enhancement mode *p*-RTGTs have been measured. Finally, the adaptive characteristics of the *p*-RTGTs have been measured in section 7.7.2.3.

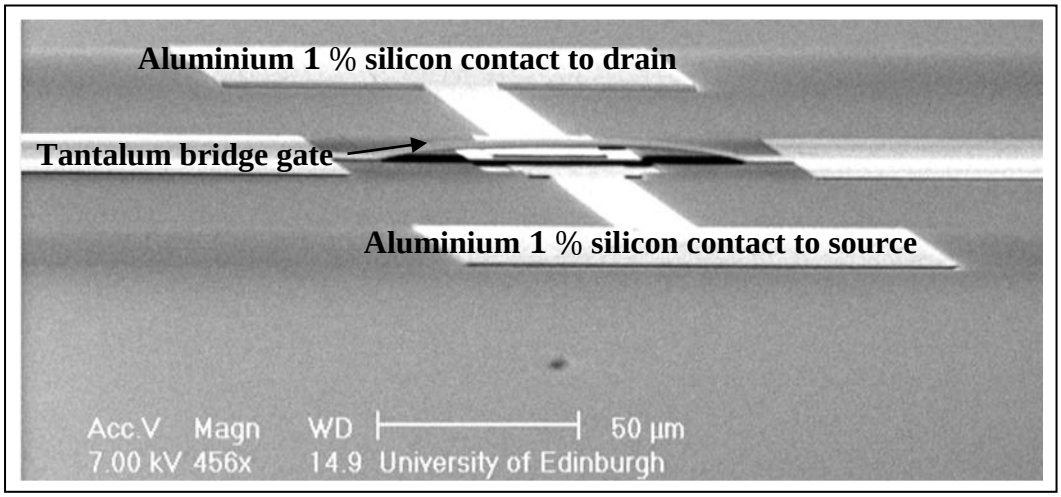
7.7.2.1 Influence of channel width on pull-in voltage and transconductance

The fabricated enhancement mode *p*-RTGTs of $l_b = 92\,\mu m$ and $l_b = 278\,\mu m$ have been measured to possess an air gap spacing of d_i~$7\,\mu m$ and d_i~$13\,\mu m$, respectively as shown in Figure 7.11. The effects of increasing the size of channel width on the pull-in voltage, threshold voltage and transconductance of the *p*-RTGTs with the bridge gate length of $l_b = 92\,\mu m$ and $l_b = 278\,\mu m$ have been measured and tabulated in Table 7.2. The channel length has been fixed to $L_c = 15\,\mu m$.

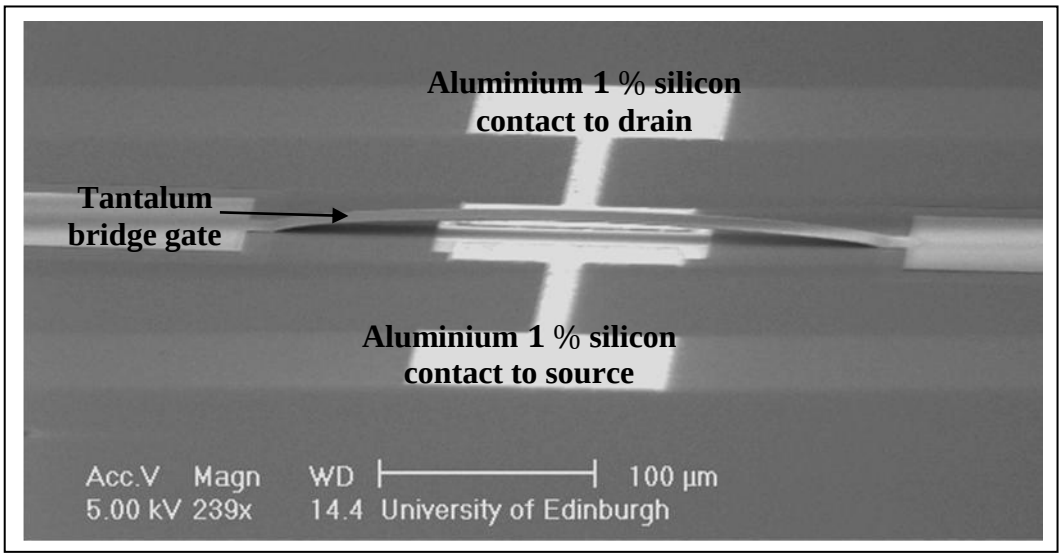
In Table 7.2, the measured transconductance at $|V_{gs}| = |V_{th}| + 14\,V$ and $V_{ds} = -10\,V$ for *p*-RTGTs of $l_b = 92\,\mu m$ increases from $2.22\,\mu S$ to $5.04\,\mu S$ as W_c increases from $40\,\mu m$ to $80\,\mu m$. The average threshold voltage of V_{th}~$-20\,V$ has been measured from the devices. The pull-in voltage for *p*-RTGTs of $l_b = 92\,\mu m$ has been measured to be greater than $100\,V$.

For *p*-RTGTs of $l_b = 278\,\mu m$, the measured transconductance increases from $27\,\mu S$ to $50.3\,\mu S$ as W_c increases from $100\,\mu m$ to $140\,\mu m$. The average threshold voltage of $V_{th} = -10\,V$ has been measured. The pull-in voltage for *p*-RTGTs of $l_b = 278\,\mu m$ has been measured to decrease from $83.6\,V$ to $80.4\,V$ with respect to the increase of W_c. For both *p*-RTGTs of $l_b = 92\,\mu m$ and $l_b = 278\,\mu m$, the increase in transconductance with respect to the increase in channel width is expected as predicted by equation 2.20. Smaller threshold voltages measured from *p*-RTGTs of $l_b = 278\,\mu m$ compared to the *p*-RTGTs of $l_b = 92\,\mu m$ are unexpected since the air

gap spacing is larger for *p*-RTGTs of $l_b = 278\ \mu m$. Based on the threshold voltage measurement in section 7.4.2, the increase of air gap spacing has been deduced to increase the threshold voltage of the device.



(a) $l_b = 92\ \mu m$



(b) $l_b = 278\ \mu m$

Figure 7.11 *The SEM micrograph images of the fabricated p-RTGTs with channel length of $L_c = 15\ \mu m$. (a) The tantalum bridge gate of $l_b = 92\ \mu m$ with the channel width of $W_c = 40\ \mu m$ possesses an air gap spacing of d_i~7 μm while (b) $l_b = 278\ \mu m$ with $W_c = 100\ \mu m$ possesses d_i~13 μm.*

Therefore, smaller threshold voltages measured from *p*-RTGTs of $l_b = 278\ \mu m$ compared to the *p*-RTGTs of $l_b = 92\ \mu m$ might be related to the electromechanical deflections of the tantalum bridge gates for *p*-RTGTs of $l_b = 278\ \mu m$ with respect to the applied V_{gs}. In contrast, insignificant electromechanical deflections for *p*-RTGTs of $l_b = 92\ \mu m$ have been measured. The tantalum bridge gate structures for *p*-RTGTs of $l_b = 278\ \mu m$ deflected and the air gap spacing probably decreased from d_i~13 μm to $d_i < 7\ \mu m$. The decrease in distance from the tantalum bridge gate to the channel has reduced the threshold voltage for *p*-RTGT of $l_b = 278\ \mu m$.

l_b	92 μm			278 μm		
d_i	7 μm			13 μm		
$W_c\ (\mu m)$	40	60	80	100	120	140
$g_m\ (\mu S)$	2.22	4.14	5.04	27.0	49.8	50.3
$V_{th}\ (V)$	-20	-20	-20	-10	-10	-10
$\lvert V_{pi} \rvert (V)$	> 100	> 100	> 100	83.6	82.8	80.4

Table 7.2 *The increase in W_c increases the transconductance and decreases the pull-in voltage of the enhancement mode p-RTGTs.*

In Table 7.2, the decrease of pull-in voltage V_{pi} with respect to the increase in W_c measured from *p*-RTGTs of $l_b = 278\ \mu m$ is related to the increase of the channel area, $W_c \times L_c$ as shown by equation 7.6. The tantalum bridge gate experiences greater electrostatic force from the channel with larger area.

$$V_{pi} \propto \sqrt{\frac{{d_i}^3}{(W_c \times L_c){l_b}^3}} \tag{7.6}$$

The length of tantalum bridge gate structure has been found to be the dominant factor that determines the pull-in voltage of *p*-RTGT. Higher V_{pi} has been measured for *p*-RTGTs of $l_b = 92\ \mu m$ compared to $l_b = 278\ \mu m$. Even though the distance d_i from the channel to the bridge gate for $l_b = 92\ \mu m$ is smaller than $l_b = 278\ \mu m$, the shorter length of the bridge gate structure has caused the pull-in voltage to be higher.

Further investigations on the effects of increasing the bridge gate length from $0.57\ mm$ to $1.62\ mm$ on the threshold voltage and pull-in voltage of the *p*-RTGTs have been presented in the next section. Overall, the increase in channel width for the enhancement mode *p*-RTGTs has 1) increase the transconductance and 2) decrease the pull-in voltage.

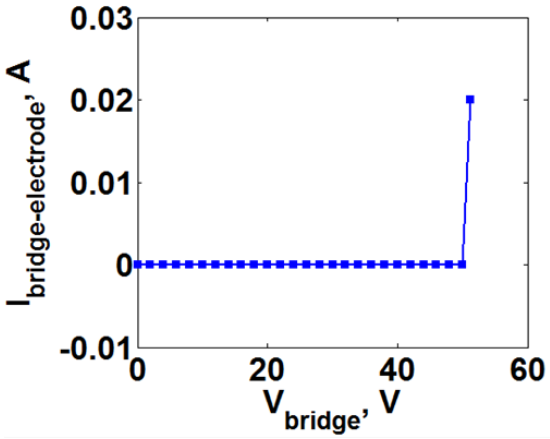
7.7.2.2 Influence of bridge gate length on pull-in voltage and threshold voltage

In order to measure the pull-in voltage of the enhancement mode *p*-RTGTs with the bridge gate length of $l_b = 0.57\ mm - 1.62\ mm$, test structures have been fabricated. In the test structure, the electrode pad of similar dimensions with the channel area of *p*-RTGT has been created underneath the tantalum bridge. The pull-in voltage V_{pi} has been measured from the tantalum bridge structure by biasing the bridge with a DC voltage and grounding the electrode pad. The exerted attractive electrostatic force between the bridge and the electrode pad will deflect the bridge towards the substrate.

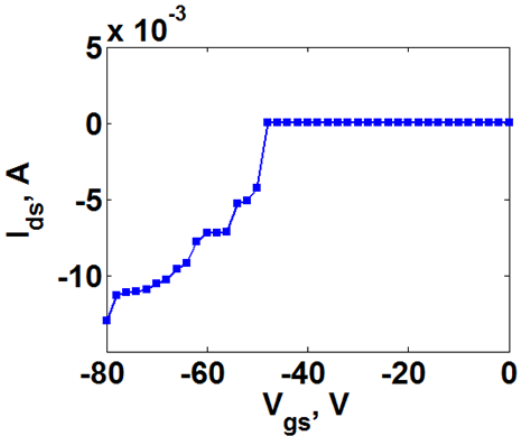
The measurement of the pull-in voltage from the test structure of $l_b = 0.72\ mm$ is shown in Figure 7.12(a). The applied voltage onto the tantalum bridge V_{bridge} has been increased and the current flow from the bridge to the electrode pad $I_{bridge-electrode}$ has been measured. The bridge is considered to be under a pull-in condition when the bridge is making a physical contact with the electrode pad. This is indicated by the sudden large of current flow measured from the bridge to the electrode pad due to the contact. For tantalum bridge of length $l_b = 0.72\ mm$, V_{pi} has been measured to be $\sim 51.2\ V$.

The pull-in voltage can also be measured directly from the enhancement mode *p*-RTGT as shown in Figure 7.12(b). At a constant drain to source voltage V_{ds}, the applied voltage onto the tantalum bridge gate V_{gs} has been increased and the current flow I_{ds} between source and drain has been measured. The sudden high I_{ds} current flow indicates a pull-in condition. For *p*-RTGT of $l_b = 0.72\ mm$, $|V_{pi}|$ has been

measured to be $\sim 50\,V$. The measured pull-in voltages using both methods agree fairly well with each other.



(a) Pull-in measurement from the test structure

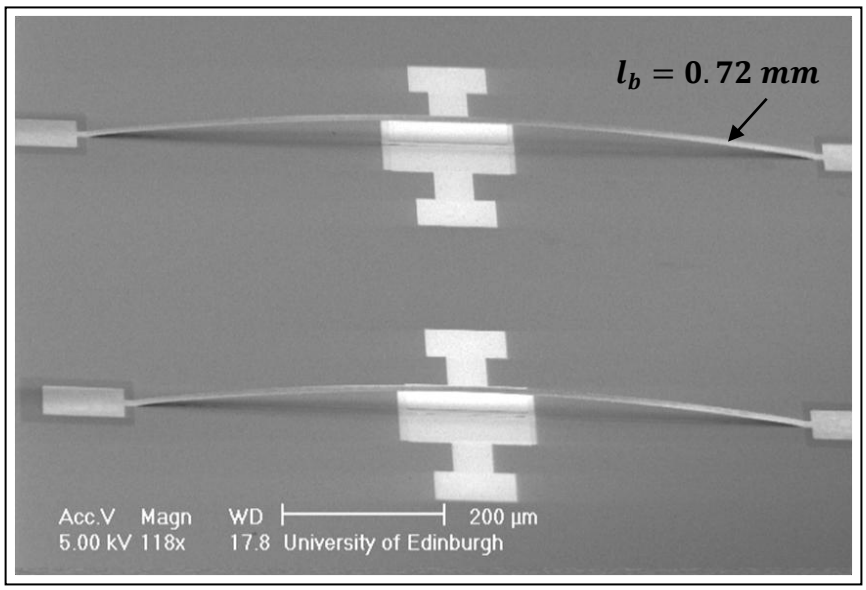


(b) Pull-in measurement from the *p*-RTGT

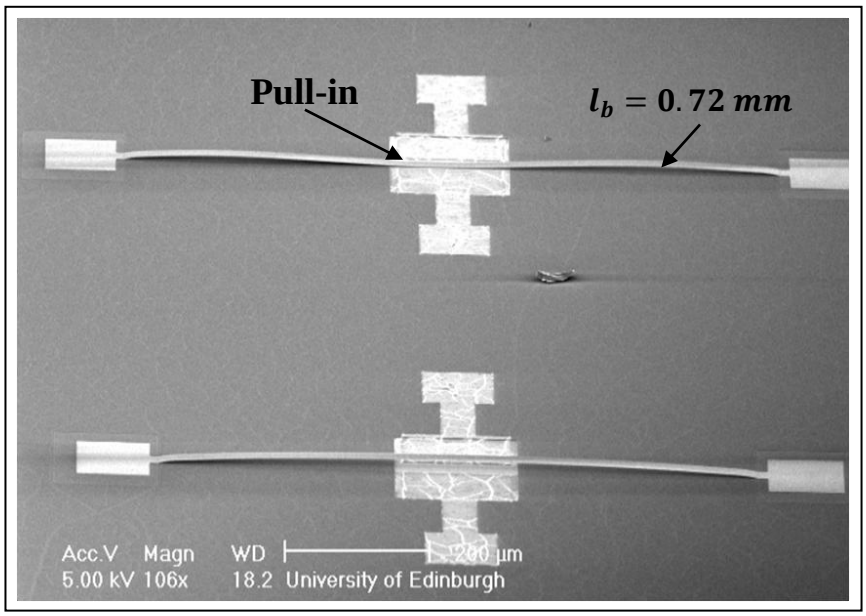
Figure 7.12 *(a) The measurement of current flow from the tantalum bridge of $l_b = 0.72\,mm$ to the electrode pad as the voltage applied onto the bridge increases. (b) The measurement of current flow between drain and source for the enhancement mode p-RTGT of $l_b = 0.72\,mm$ as the voltage applied onto the bridge gate increases. The pull-in condition occurred when high current is detected during a physical contact between the bridge/bridge gate and the electrode pad/channel region. The pull-in voltage has been measured to be $\sim 51.2\,V$ from (a) and $\sim 50\,V$ from (b).*

The SEM micrograph images in Figure 7.13 show the conditions of the *p*-RTGT of $l_b = 0.72\,mm$ before and after the pull-in voltage measurement. During the pull-in

contact, the applied high voltage onto the tantalum bridge gate has been observed to break down the thin gate oxide layer and destroy the channel underneath. Thus, the pull-in voltage measurement using the test structures is preferable.



(a) Before measurement



(b) After measurement

Figure 7.13 *The SEM micrograph images of the fabricated p-RTGT of* $l_b = 0.72\ mm$ *(a) before and (b) after the pull-in voltage measurement.*

The measured pull-in voltage and threshold voltage for the enhancement mode *p*-RTGTs of $l_b = 0.57\,mm - 1.62\,mm$ are tabulated in Table 7.3. The devices are labelled as $B10 - B1$ with respect to the increase in bridge gate length l_b. The channel area underneath the bridge gate has been fixed to $20\,\mu m \times 160\,\mu m$. As the bridge gate length increases from $l_b = 0.57\,mm$ to $1.62\,mm$, the air gap spacing before the pull-in voltage measurement has been measured to increase from d_i~$20.1\,\mu m$ to $58.3\,\mu m$.

Label	l_b, mm	$d_i, \mu m$	$\lvert V_{pi}\rvert, V$	$\lvert V_{th}\rvert, V$
$B10$	0.57	20.1	60.5	30
$B9$	0.64	23.0	52.5	30
$B8$	0.72	25.9	50.0	31
$B7$	0.81	31.5	49.0	33
$B6$	0.91	34.4	48.5	40
$B5$	1.02	37.2	43.5	n/a
$B4$	1.14	40.2	41.5	n/a
$B3$	1.28	46.4	36.5	n/a
$B2$	1.44	51.9	33.0	n/a
$B1$	1.62	58.3	30.5	n/a

Table 7.3 *The increase in bridge gate length l_b reduces the pull-in voltage $\lvert V_{pi}\rvert$ while the increase in air gap spacing d_i increases the threshold voltage $\lvert V_{th}\rvert$ of the enhancement mode p-RTGTs.*

In equation 7.6, the increase in bridge gate length l_b will reduce the pull-in voltage. On the other hand, the increase in air gap spacing d_i gives an opposite effect of increasing the pull-in voltage. From the measurement results in Table 7.3, the pull-in voltage has decreased from $\lvert V_{pi}\rvert = 60.5\,V$ to $30.5\,V$ for $B10 - B1$. Thus, the influence of bridge gate length l_b on the pull-in voltage dominates over the influence of air gap spacing d_i.

In Table 7.3, the threshold voltage has been measured to increase from $|V_{th}| = 30\,V$ to $40\,V$ as the bridge gate length increases from $l_b = 0.57\,mm$ to $0.91\,mm$, due to the increase in the air gap spacing. In section 7.5, the increase in air gap spacing has been deduced to increase the threshold voltage of the device. For the enhancement mode *p*-RTGTs of $l_b = 1.02\,mm - 1.62\,mm$, the devices have not been turned on and no modulation has been measured. This is because the threshold voltage for the *p*-RTGTs of $l_b = 1.02\,mm - 1.62\,mm$ is higher than the pull-in voltage. Therefore, the safe operating limit for the applied voltage onto the tantalum bridge gate of *p*-RTGT should satisfy $|V_{th}| < |V_{gs}| < |V_{pi}|$.

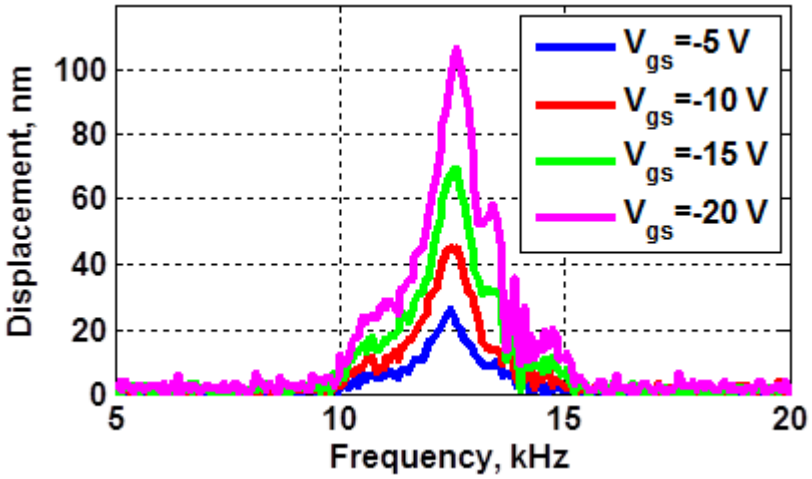
7.7.2.3 Adaptive characteristics of the tantalum bridge gate

In this section, the adaptive behaviour of the tantalum bridge gate structures within the audible frequency range has been demonstrated. The fabricated enhancement mode *p*-RTGTs with the tantalum bridge gate $B6$ of length $l_b = 0.91\,mm$ and $B5$ of length $l_b = 1.02\,mm$ have been actuated electrostatically by applying the AC voltage of $10\,V$ peak to peak onto the tantalum bridge gates.

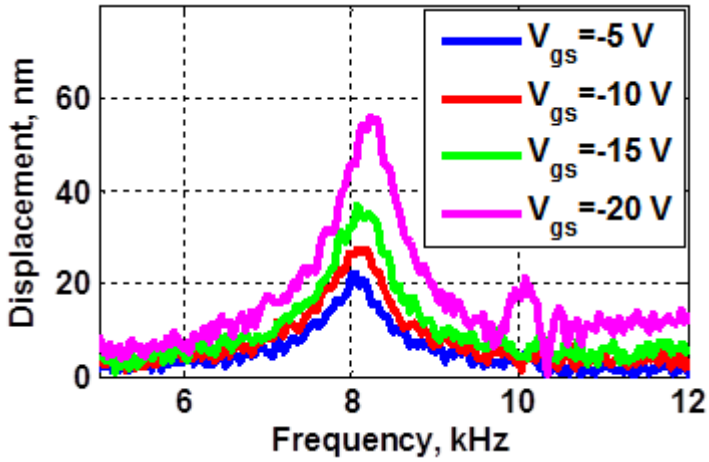
The frequency measurements have been carried out using the laser vibrometer in the standard atmospheric pressure of $\sim 760\,mTorr$. The applied DC voltage onto the bridge gate with respect to source V_{gs} has been increased from $-5\,V$ to $-20\,V$ while the applied DC voltage between source and drain V_{ds} has been fixed at $-5\,V$. The exerted alternating electrostatic force between the tantalum bridge gate and channel has caused the bridge to vibrate.

In section 4.4.3, the smallest measured frequency from the buckled tantalum bridge has been found to be the second mode of the bridge. In Figure 7.14, the measured second mode for the buckled tantalum bridge gate $B6$ and $B5$ are $f_2 \sim 12.6\,kHz$ and $f_2 \sim 8.5\,kHz$ with the quality factor of $Q_{10} \sim 5.4$ and $Q_{10} \sim 4.7$, respectively. For the RGT cochlear biomodel application, the measured responses from the fabricated buckled tantalum bridge gates operating in air are fairly acceptable and close to the

responses from the basilar membrane measured by others with the quality factors of Q_{10}~$0.6 - 10$ and vibration displacements in $2\ nm - 20\ nm$ range [5][6].



(a) $B6$ of length $l_b = 0.91\ mm$



(b) $B5$ of length $l_b = 1.02\ mm$

Figure 7.14 *The adaptive characteristics i.e self-tuning ability of the tantalum bridge gates in p-RTGT devices. The vibration displacements for the tantalum bridge gate (a) $B6$ of length $l_b = 0.91\ mm$ and (b) $B5$ of length $l_b = 1.02\ mm$ increased with respect to the increase in bridge gate voltage. The second mode of the tantalum bridge gate is stable towards the changes of the applied bridge gate voltage.*

In Figure 7.14, the self-tuning characteristics of the *p*-RTGT devices have been demonstrated by the increase of the bridge gate displacement with respect to the

increase in the bridge gate voltage. With the increase of V_{gs} from $-5\,V$ to $-20\,V$, the amplitude increases to $\sim 2.5-4$ times greater. In contrast, the second mode has been measured to be constant with respect to the bridge gate voltage. The tantalum bridge gate in *p*-RTGT possesses high frequency stability.

As has been described from the mathematical model of RGT in section 2.4.4.2 in Chapter 2, the elastic restoring coefficient k of the bridge gate varies with respect to V_{gs}. Therefore, the vibration displacement of the bridge gate structure can be tuned simply by varying the applied bridge gate voltage. The self-tuning ability of each individual bridge gate structure is desired for the adaptive RGT cochlear biomodel application.

7.8 Conclusion

In this chapter, the enhancement mode *p*-MOSFETs and *p*-RTGTs have been fabricated. In the fabrication of these *p*-channel devices, boron implantation for source/drain regions has been performed after the growth of gate oxide layer in order to prevent the segregation of boron dopants from silicon substrate to the grown gate oxide layer. The high subthreshold current issue occurred within the *n*-channel devices in Chapter 6 has been solved by employing the *p*-channel devices. 100 % of the fabricated enhancement mode *p*-channel devices can be turned off at low values of subthreshold currents. The influence of positive oxide charges Q_{ss} that induces the high subthreshold current has been reversed and eliminated by the use of *p*-channel devices. However, the measured drain current from the *p*-MOSFETs have been found to be one order smaller compared to the *n*-MOSFETs, indicating the smaller effective surface mobility of holes in *p*-channel devices compared to the electrons in *n*-channel devices.

Comparing the measurement from *p*-RTGT of bridge gate length $l_b = 92\,\mu m$ with its *p*-MOSFET equivalent, the transconductance for *p*-RTGT has been measured to be one order less while the threshold voltage is one order higher, due to the effect of introducing an air gap layer of $\sim 7\,\mu m$ thickness on top of the $70\,nm$ thickness of

gate oxide layer. The analytical models of drain current for the *p*-MOSFET and *p*-RTGT have been studied. By fitting the models to the measurement data, the effective surface holes mobility of the device has been estimated to be $\mu_h = 200\ cm^2/Vs$ while the total capacitance between the channel and the tantalum bridge gate of *p*-RTGT has been estimated to be $C_{total} = 1.0\ \mu F/m^2$. The smaller C_{total} for *p*-RTGT compared to the *p*-MOSFET quantifies the smaller transconductance measured from *p*-RTGT. From the analytical threshold voltage model of *p*-MOSFET, the built-in positive oxide charges have been estimated to be $Q_{ss} = q(1.6e^{12})\ cm^{-2}$ which is higher compared to the estimated Q_{ss} in *n*-MOSFET. Higher Q_{ss} has been postulated to induce the formation of stronger electrons inversion layer within the silicon channel surface which will then increase the reverse effect in *p*-MOSFET devices.

The effect of increasing the channel width W_c and decreasing the channel length L_c of the enhancement mode *p*-MOSFETs has been found to increase the transconductance g_m of the device. Similar trend of increase in the transconductance with respect to W_c has been measured from the enhancement mode *p*-RTGTs. The pull-in voltage $|V_{pi}|$ of the enhancement mode *p*-RTGTs has been found to decrease with the increase of W_c, due to the increase of the exerted attractive electrostatic force from the bigger channel area, $W_c \times L_c$.

The bridge gate length l_b has been found to be the dominant factor that determines the pull-in voltage of the enhancement mode *p*-RTGT. In addition, the air gap spacing d_i has been found to influence the threshold voltage $|V_{th}|$. As the tantalum bridge gate length increases from $l_b = 0.57\ mm$ to $1.62\ mm$, the air gap spacing increases from $d_i \sim 20.1\ \mu m$ to $58.3\ \mu m$. The pull-in voltage has been measured to decrease with respect to the increase in bridge gate length while the threshold voltage has been measured to increase with respect to the increase in air gap spacing. For *p*-RTGTs of $l_b \geq 1.02\ mm$, the threshold voltage of the channel has been found to be higher than the pull-in voltage of the tantalum bridge gate, leading to the failure operation of the *p*-RTGT device. The safe operating limit of the voltage to be

applied onto the tantalum bridge gate of the enhancement mode *p*-RTGTs has been deduced to be $|V_{th}| < |V_{gs}| < |V_{pi}|$. Finally, the self-tuning ability of the enhancement mode *p*-RTGTs within the audible frequency range has been demonstrated by the increase in the tantalum bridge gate displacement with respect to the increase in the applied bridge gate voltage.

Chapter 8: Conclusion

The thesis has presented the theoretical and fabrication development of the resonant gate transistors (RGTs) for the adaptive RGT cochlear biomodel application. Significant characterisation and analysis on the mechanical behaviour and electrical static response of the RGTs have been made. These will contribute to the fabrication of a reliable RGT device suited for the cochlear biomodel application. In this chapter, the main conclusion on the fabrication and performance of the RGT devices will be discussed.

8.1 Theoretical development of RGT cochlear biomodel

The RGT device has been designed and employed in our cochlear biomodel. In the RGT cochlear biomodel, an array of RGTs has been considered which consists of 1) the mechanical bridge gate structures for sound-vibration transduction and 2) the channel region with source/drain for vibration-electrical transduction.

In Chapter 2, the mathematical model for RGT has been developed to mimic the cochlea. From the mathematical model, 1) the employment of bridge gate structures with different length has been found to mimic the frequency-to-place mapping characteristics of the basilar membrane within the cochlea. 2) The estimated electromechanical response of RGT with respect to the applied DC voltage onto the bridge gate structure reveals the device's potential of mimicking the adaptive behaviour of human cochlea. 3) The estimated electrical output from RGT has been found to be comparable with the frequency response measured from the hair cells within the cochlea. The detailed design and specification for the RGT device have been presented in Chapter 2.

The spike event coded RGT-cochlear system has been proposed which integrates the adaptive RGT cochlear biomodel with the spike interface neuromorphic circuit and Address Event Representation protocol (AER) system buses for the development of the neuromorphic auditory system. The estimated electrical output from RGT cochlear biomodel has been tested with the spike encoder prototype circuits and has been found to be suitable for neural spike coding. Thus, the transformation of the electrical signals from cochlea into neural spikes can be copied.

8.2 Development of bridge gate structures for RGT

From the design consideration in Chapter 2, aluminium and tantalum metal layer have been chosen as the material structures for the bridge gate of RGT. Arrays of bridge gates with length $l_b = 0.57\ mm - 5.8\ mm$ have been designed in order for the device to work within the audible frequency range $f_1 = 51\ Hz - 8\ kHz$.

In Chapter 3, the fabrication steps to create the bridge gate structure have been developed. In order to create a free-standing bridge gate structure which is supported by two anchors, the photoresist sacrificial layer has been used to suspend the bridge gate above the substrate. Then, the bridge gate structures have been released from the photoresist sacrificial layer using an etch release process. The downstream oxygen/nitrogen plasma etch release technique has been developed and found to be able to offer a clean, reliable and damage-free etch release process for the bridges.

From the characterisations of the etch release process, the etch rate has been found to increase with the increase of substrate temperature and oxygen/nitrogen gas flow rates. Thus, the etch release process for releasing the aluminium and tantalum bridge gate structures from the photoresist sacrificial layer has been optimised to high substrate temperature of $250\ °C$ and considerably high oxygen/nitrogen gas flow rates of $2500\ sccm/500\ sccm$.

In Chapters 3-4, the profiles of the released aluminium and tantalum bridge gates have been monitored and the biaxial residual stress within the structures have been analysed.

8.2.1 Characterisation of aluminium bridge gate structure

In Chapter 3, the aluminium bridge gate structures have been fabricated. The sputter-deposition and reactive ion etching of aluminium are faster and more straightforward compared to tantalum. The released aluminium bridge gates of length $l_b < 1\ mm$ have been observed to be free-standing. However, the released aluminium bridge gates of length $l_b > 1\ mm$ have been found to sag down and touch the substrate.

The presence of biaxial residual stress within the structures has induced the sagging and collapsing of the aluminium bridge gates. The sagged aluminium bridge gates have been postulated to be under the influence of tensile stress. The increase in bridge gate length for the tensile-stressed aluminium bridge gate has been simulated to increase the sagging of the structure. Thus, the collapsing of the aluminium bridge gate occurs as the bridge gate length continues to increase. The aluminium metal layer could not withstand the induced biaxial residual tensile stress within the bridge structure.

Next, the tantalum metal layer with better mechanical properties compared to aluminium has been considered. The tantalum metal with higher yield strength and Young's modulus can withstand the induced biaxial residual stress within the structure.

8.2.2 Characterisation of tantalum bridge gate structure

In Chapter 4, the tantalum bridge gate structures have been fabricated to be free-standing. The employment of tantalum metal as the bridge gate has solved the sagging and collapsing issues occurred in the aluminium bridge gate structure. The released tantalum bridge gates possess either the straight or buckle profile. The induced biaxial residual stress within the tantalum bridge gate has influenced the profile and the mechanical behaviour of the released structure.

The total residual stress induced within the sputter-deposited tantalum metal layer has been measured to be compressive with the estimated value of $\sim -310\ MPa$.

The subsequent processing steps to fabricate the bridge gate structure from the sputter-deposited tantalum metal layer have either increased the induced compressive stress or transformed into tensile stress.

8.2.2.1 Tensile-stressed straight tantalum bridge gate

The biaxial residual stress within the straight tantalum bridge gates has been found to be tensile. The average tensile stress for the bridge gate length of $l_b = 1.62\,mm - 0.57\,mm$ has been extracted to be $\sim 3\,MPa - 10\,MPa$. The measured lowest frequency from the bridge gate has been detected to be the first mode. The presence of tensile stress has increased the first mode of the straight tantalum bridge gates to be higher than the ideal stress-free straight tantalum bridge gates. The first modal shape has been simulated to possess the 1st symmetrical bending motion.

8.2.2.2 Compressive-stressed buckled tantalum bridge gate

The biaxial residual stress within the buckled tantalum bridge gates has been found to be compressive. The compressive stress beyond the critical buckling load for the bridge gate length of $l_b = 1.62\,mm - 0.57\,mm$ has been extracted to be $\sim -850\,MPa$. The measured lowest frequency from the bridge gate has been detected to be the second mode. The domination of curvature effect has increased the second mode of the buckled tantalum bridge gate to be higher than the ideal stress-free straight tantalum bridge gates. The second modal shape has been simulated to possess the 2nd symmetrical bending motion.

8.2.2.3 Mechanical frequency response

The lowest detected mode for the compressive-stressed buckled tantalum bridge gates i.e. the second mode of length $l_b = 5.8\,mm - 0.57\,mm$ has been measured to be $f_2 = 550\,Hz - 29.4\,kHz$. As for the tensile-stressed straight tantalum bridge gates of length $l_b = 1.62\,mm - 0.57\,mm$, the lowest detected mode i.e. the first mode of $f_1 = 4.2\,kHz - 18.8\,kHz$ have been measured. In open air with the standard atmospheric pressure of $\sim 760\,mTorr$, the vibration displacement of $\sim 0.04\,nm - 1.3\,nm$ and quality factor of $Q_{10} \sim 1 - 3$ have been achieved.

For the RGT cochlear biomodel application, the measured responses from the tantalum bridge gates are fairly acceptable and close to the responses from the basilar membrane with Q_{10}~$0.6-10$ and vibration displacement in $2\,nm-20\,nm$ range measured by others [5][6]. In addition, it is suggested that higher quality factor and vibration displacement from the tantalum bridge gates can be achieved by adjusting the air pressure to be smaller than $\sim 760\,mTorr$.

8.3 Development of channel and source/drain for RGT

The fabrication steps to create the channel and source/drain for RGT have been developed. Ion implantation technique has been carried out to form the source/drain regions. The metal-semiconductor interfacial contact between the implanted source/drain regions and metal electrode has been made through the contact windows. Aluminium 1% silicon has been employed as the metal electrode. The threshold voltage and transconductance of RGT have been found to depend mainly on the air gap spacing distance from the channel region to the bridge gate structure.

8.3.1 Characterisation of *n*-type channel and integration with aluminium and tantalum bridge gate structures

For *n*-type channel, phosphorus ions have been implanted in source/drain regions. In Chapter 5, small sheet resistivity within the phosphorus implanted source/drain regions has been achieved. In addition, the metal-semiconductor interfacial contact area between the aluminium 1% silicon metal electrode and phosphorus implanted source/drain regions has been increased in order to obtain small interfacial contact resistance. Good drain current conduction from drain to source has been achieved due to small sheet and contact resistivities.

In Chapter 6, the *n*-channel metal-oxide-semiconductor field-effect transistors (*n*-MOSFETs) have been studied for the development of the *n*-channel resonant gate transistors (*n*-RGTs). The enhancement and depletion mode *n*-MOSFETs have been fabricated and characterised. The presence of positive oxide charges Q_{ss} within the gate oxide has caused the 1) designed threshold voltage to become more negative, 2)

depletion mode characteristics for the enhancement mode devices and 3) high subthreshold current. High subthreshold current affected the devices' performance by reducing the strength in modulation of channel conductance, giving small values of transconductance.

The decrease in boron substrate doping probably due to the segregation of boron has been postulated to be the first order effect that influenced Q_{ss} to induce stronger electrons inversion layer within the channel of *n*-MOSFETs, leading to higher subthreshold current and in the worst case scenario, the channel breakdown. The second order effect has been found to be the domination of the electric field from drain voltage over the perpendicular electric field from gate voltage on the channel. In order to reduce the second order effect, 1) channel length has been increased, 2) furnace temperatures used in the fabrication of *n*-MOSFETs have been reduced and 3) thinner gate oxide layer has been grown. These optimisations have minimised the subthreshold current and eliminated the occurrence of channel breakdown within *n*-MOSFETs. In *n*-RGT device however, the influence of the perpendicular electric field from the bridge gate is smaller due the presence of air gap layer. Thus, the second order effect has not been minimised in *n*-RGT and high subthreshold currents have been measured.

Aluminium and tantalum bridge gates have been integrated with the enhancement mode *n*-type channel and source/drain regions to form the enhancement mode *n*-channel resonant aluminium gate transistor (*n*-RAGT) and *n*-channel resonant tantalum gate transistor (*n*-RTGT), respectively. The presence of air gap layer in *n*-RAGT and *n*-RTGT caused 1) the transconductance to be one order less than *n*-MOSFET, indicating smaller modulation of channel conductance and 2) the threshold voltage to be one order higher than *n*-MOSFET, indicating higher bridge gate voltage is needed to turn the device on/off.

The *n*-RAGT has been deflected electromechanically by the voltage applied onto the aluminium bridge gate structure and thus the air gap spacing has reduced. For *n*-RTGT of similar length, higher mechanical restoration force of the tantalum bridge

gate structure and larger air gap spacing have caused insignificant electromechanical deflection of the device. Due to smaller air gap spacing, *n*-RAGTs possess higher transconductance than *n*-RTGTs. Larger electromechanical deflection for *n*-RTGT has been achieved by using 1) bigger channel width and 2) longer bridge gate structure.

8.3.2 Characterisation of *p*-type channel and integration with tantalum bridge gate structure

In Chapter 7, the presence of high subthreshold current in *n*-RGT has been removed by employing the *p*-type channel. For *p*-type channel, boron ions have been implanted in source/drain regions and the influence of positive oxide charges Q_{ss} on the channel has been reversed. The *p*-channel resonant gate transistors have been measured with better modulation of channel conductance compared to the *n*-channel resonant gate transistors.

The *p*-channel metal-oxide-semiconductor field-effect transistors (*p*-MOSFETs) have been developed for the *p*-channel resonant gate transistors (*p*-RGTs). The enhancement mode *p*-type channel and boron implanted source/drain regions have been integrated with the tantalum bridge gate structure, forming the enhancement mode *p*-channel resonant tantalum gate transistor (*p*-RTGT).

The influence of air gap layer in *p*-RTGT has been modelled to decrease the total capacitance between the channel and bridge gate, making the transconductance of the *p*-RTGT devices to be one order less than *p*-MOSFET. The pull-in voltage of the enhancement mode *p*-RTGT decreased with the increase of bridge gate length while the threshold voltage increased. At certain bridge gate length, the threshold voltage became higher than the pull-in voltage. The designed pull-in voltage for *p*-RTGT has to be higher than the threshold voltage in order for the device to work. Finally, the *p*-RTGTs have been shown to be able to self-tune the vibration displacements of the tantalum bridge gate structures within the audible frequency range.

8.4 Further work

The next steps will be to 1) measure the AC drain current response from the fabricated RGT, 2) examine the adaptive characteristics of the device from the measured drain current and 3) integrate the fabricated device with the spike interface neuromorphic circuit. Even though the fabricated RGT has not been integrated with the spike interface neuromorphic circuit as described in the proposal, significant contributions have been made in developing the RGT device for cochlear biomodel application.

In this work, the modulations of channel conductance for both *n*-RGT and *p*-RGT devices have been obtained. Although the drain current output from the fabricated *p*-RGT devices are smaller than *n*-RGT due to the smaller effective surface mobility of holes, *p*-RGT demonstrates better output characteristics with small subthreshold current. The design of RGT can be further optimised in order to increase the transconductance and decrease the threshold voltage. The threshold voltage needs to always be smaller than the pull-in voltage in order for the device to work. This can be achieved by decreasing the distance of the bridge gate structure from the channel region. The decrease in pull-in voltage has to be compromised accordingly.

Tantalum has been seen as a promising material structure for the bridge gate of RGT. The fabricated tantalum bridge gates operate within the audible frequency range with the vibration displacement and quality factor close to the specification design of our RGT cochlear biomodel. In addition, the adaptive characteristics have been achieved from the tantalum bridge gates. The profile of the fabricated tantalum bridge gate however is inconsistent as the released structure demonstrates either a straight or buckle behaviour.

The buckled bridge gate structure with upwards deflection changed the initial design of the air gap spacing distance from the bridge gate to channel region and subsequently affects the designed threshold voltage of RGT. In addition, the upwards deflection increased with the increase of bridge gate length, adding more variation in the threshold voltage. In order to gain control in designing the threshold

voltage of RGT, straight bridge gates are desired. The air gap distance can then be controlled and become consistent with respect to the bridge gate length.

Additional material layers can be deposited onto the bridge gate to straighten the buckling structure. First, the induced stress within the buckled structure is estimated. Then, the additional material layers with thickness and stress that can compensate the buckling structure are deposited [112][113]. Similarly, the sagged aluminium structure can also be made straight by depositing the additional material layers that can compensate the sagging. The geometrical design of the multilayer bridge gate structure needs to be optimised and compromised accordingly in order to operate within the audible frequency range.

New structures can be employed to substitute the bridge gate in RGT. Complex MEMS resonator shapes like crab-legged and serpentine which possess small elastic restoring coefficient/spring constant can be designed to work within the audible frequency range [Figure 8.1][24]. In fact, the resonant frequencies for the crab-legged and serpentine structures of similar length with the bridge gate have been simulated to be ~ 2 and ~ 12 times smaller than the bridge gate. Thus, smaller length of MEMS resonator can be fabricated for the RGT.

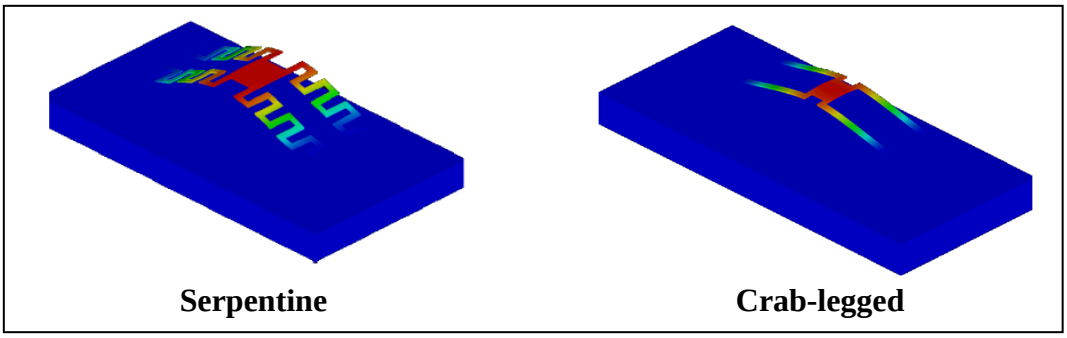


Figure 8.1 *Crab-legged and serpentine structures can operate at the resonant frequencies of ~ 2 and ~ 12 times smaller than the bridge gate structure of the same length.*

In addition, the resonant frequency for the MEMS resonator can be further reduced to cover the lower frequency region in the audible spectrum without having to increase the structural length. Platinum can be deposited at the middle section of the

MEMS resonator structure using the focused ion beam (FIB) technique [114]. The increase in effective mass of the structure reduces the resonant frequency.

8.5 Publication

Some of the work carried out in the thesis have been published in relevant journal and conference proceeding. The publications are listed in the chronological order;

R. Latif, E. Mastropaolo, A. Bunting, R. Cheung, T. Koickal, A. Hamilton, M. Newton, and L. Smith, "Microelectromechanical systems for biomimetical applications", *Journal of Vacuum Science and Technology B*, vol. 28, no. 6, pp. C6N1-C6N6, 2010.

T. Koickal, R. Latif, L. Gouveia, E. Mastropaolo, S. Wang, A. Hamilton, R. Cheung, M. Newton, and L. Smith, "Design of spike event coded RGT microphone for neuromorphic auditory systems," *IEEE International Symposium on Circuits and Systems*, Rio de Janeiro, Brazil, pp. 2465-2468, 15-18 May 2011.

R. Latif, E. Mastropaolo, A. Bunting, R. Cheung, T. Koickal, A. Hamilton, M. Newton, and L. Smith, "Low frequency tantalum electromechanical systems for biomimetical applications", *Journal of Vacuum Science and Technology B*, vol. 29, no. 6, pp. 06FE05/1-06FE05/6, 2011.

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